National Center for Scientific Research:
NCSR "Demokritos"

NCSR Demokritos
Institute of Microelectronics

Annual Report 2006

Aghia Paraskevi, Athens, Greece
www.imel.demokritos.gr

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MAIN RESEARCH RESULTS

PREFACE

IMEL (Institute of Microelectronics) has been established in the year 1986 as one of the eight Research Institutes of NCSR Demokritos (National Center for Scientific Research), a medium size, multidisciplinary Research Center under the General Secretarial for Research and Technology of the Ministry of Development.

Through more than 20 years of research and technology, IMEL has developed experience and expertise, as well as unique technological advantages, which place it among the main EU Research Institutes in the field of Silicon technologies.

Its initial focus on Microelectronics has been expanded to the fields of sensors and MEMs/NEMs, including nano-biosensors and systems. The strong advantages of IMEL are as follows:

- Its excellent staff, composed of a small number of experienced senior scientists, surrounded by a large number of young researchers, all fully devoted to their work
- Research facilities in silicon processing, micro and nanofabrication, characterization and testing, which are unique in Greece
- Important expertise and know-how, as well as important proprietary technologies, materials and devices. Its intellectual property (IP) portfolio continues to expand and opens important possibilities for collaboration with industry and transfer of know how

Research at IMEL is carried out at EU level through its participation in European research projects, networks of excellence, and technology platforms. EU projects are across a number of specific priorities of the EU Research Framework Programme, including mainly Information Society Technologies (IST), Nanotechnology, Materials and Production Processes (NMP), Energy and Health. IMEL's success in the above peer reviewed R&D funded programmes represents one of the strongest endorsements of IMEL's R&D competence and reflects the world-class standing of the Institute.

On national level the expertise and infrastructure of IMEL are unique in Greece, which makes its role for the country also unique in an effort to develop novel technologies, to transfer technology and know-how to the industry and to develop human potential, which constitutes the principal driving force for an industrial activity in high technology. Furthermore, IMEL developed mechanisms to promote the field at national level through the establishment and coordination of thematic networks and scientific societies (MMN Network, Micro & Nano scientific society).

In the year 2006 IMEL became a partner of the European Integrated Activity of Excellence and Networking for Nano and Micro-Electronics Analysis that started in December 2006 with EU funding. Through this Network IMEL provides services in advanced electrical and optical characterization of Si devices, materials and structures.

Two other strategic decisions were also taken in the year 2006. IMEL became one of the founding members of the European Academic and Scientific Association for Nanoelectronics (EASAN) that aims at promoting scientific collaborations with industry and providing skills and expertise for the execution of common projects, studies, as well as education and training in Nanoelectronics. In addition, IMEL signed a memorandum of collaboration with TYNDALL (Ireland), VTT (Finland) and CNM (Spain) to promote the field of "Beyond Moore" activities within the technology platform ENIAC for Nanoelectronics.

In this annual report, the research and education activities of IMEL are presented, together with the main achievements and results in the year 2005.

Dr A. G. Nassiopoulou
Director of IMEL
Member of the Board of Management
of NCSR Demokritos

IMEL at a glance

IMEL is one of the eight research Institutes of the multidisciplinary research center "NCSR Demokritos" in Aghia Paraskevi, a suburb situated 10 kilometers from the center of Athens.

Main Objectives of IMEL

The main objectives of IMEL are as follows:

- Long-term research into understanding phenomena, mastering processes and developing research tools.
- Development of fundamental knowledge
- Development of novel high added-value technology products and production processes
- Development of human potential by education and training activities
- Services in advanced technology
- Transfer of technology and know-how

The objectives of IMEL are in line with the government policy to promote excellence in research, high technology development and innovation at Research Institutes and to promote collaboration between academia and industry.

The objectives of IMEL are also in line with the European policy to maintain and increase EU competitiveness and sustainable development through design, development and dissemination of advanced technologies, including micro and nanotechnologies and systems. They are also in line with the EU objective to "achieve a critical mass of capacities needed to develop and exploit leading edge technologies for the knowledge- and intelligence-based products, services and manufacturing processes of the years to come".

Due to the existing infrastructure available at IMEL for silicon processing and micro- nanofabrication and the existing expertise and know-how developed, the role of the Institute is significant in contributing to increase the technological level of the country and to spread the knowledge through collaboration with Academia in research and education activities.

Research orientation

IMEL is mainly devoted to silicon technologies and their diverse applications in information processing, storage, transmission systems and telecommunications, environmental systems, medicine, healthcare, food industry etc.

Research Activities at IMEL are structured in 3 programmes, each of them being composed of smaller projects. A scientist is in charge of each research project, while a program representative is assigned for the management of each programme. The 3 programmes and the corresponding projects are as follows:

A. MICRO AND NANOFABRICATION
   - ➢ Lithographic Polymers and Processes

- ➢ Plasma Processing and Simulation for Micro and Nano Patterning
- ➢ Front-end Processes for Micro and Nanodevices
- ➢ Thin Films by Chemical Vapor Deposition (CVD)

B. NANOSTRUCTURES and NANOELECTRONIC DEVICES

- ➢ Nanostructures for Nanoelectronics and Photonics
- ➢ Silicon Nanocrystal Memories
- ➢ Molecular Materials as Components of Electronic Devices

C. SENSORS and MEMS

- ➢ Porous Silicon Technology for Sensors and on-chip Integration
- ➢ Mechanical & Chemical Sensors
- ➢ Bio-microsystems
- ➢ Thin Film Devices for Large Area Electronics
- ➢ Circuits and Devices for Optoelectronic Interconnections

The field of activities of IMEL is of paramount importance worldwide. Microelectronics has become a foremost driver of social and economic progress. The move to nano-scale devices, called nanoelectronics, further revolutionizes applications. The technologies developed at IMEL are necessary both in establishing a distinct and recognized role for the Institute at a European and international level and in supporting the national policies. More specifically:

Micro and nanofabrication

Research in this field is essential in supporting the development of microelectronics technology, where miniaturization plays a dominant role, pushing to the development of new materials and processes allowing the fabrication and proper functioning of the miniaturized devices.

Novel specific processes and schemes, and related materials, are also needed in the area of sensors and microsystems. Furthermore, the recent expansion of the broader field of Nanotechnology, referring not only to the fabrication of novel electronic and photonic devices but also to a large number of applications in areas such as biotechnology, medicine, health care, materials, environment, pushes strongly among others to the development of novel micro-nano fabrication routes suitable for these emerging applications. The expertise of IMEL researchers and its infrastructure provide the basis for the involvement in this emerging attractive field and significant results have been already demonstrated. The activity in this area enhances the impact of the Institute in the national research environment through collaboration with groups from other fields (e.g. biology, chemistry, medicine) that need support in order to launch and/or continue research effort to this exciting direction.

Nanostructures and nanoelectronic devices

The driving force in this program is the increasing need worldwide for technological innovations in Information and Communication Technologies (ICT) involving R&D which evolves more and more towards an atomic or molecular scale. The major objective in either pursuing Moore's law or finding alternative solutions is to further increase the performance of circuits within a given volume, to decrease power consumption for a given level of performance and to decrease cost.

Research at IMEL is carried out within EU projects and it aims at scientific and technological excellence and innovation, in collaboration with EU industrial partners. The importance of this activity for the country comes from the need to follow advanced technologies, to maintain the level of knowledge in this field, to support education, to spread the knowledge, to promote awareness of worldwide scientific and technological development and to promote applications.

Sensors and MEMs

The activity on sensors and MEMs is of strategic importance both for the country and for Europe. MEMs products have a number of distinguishing attributes that make them attractive for the advanced manufacturing industry of the coming century. These include:

- Suitability for low cost, high volume production
- Reduced size, weight and energy consumption
- High functionality
- Improved reliability and robustness
- Biocompatibility

This activity at IMEL started at the early nineties and the Institute develops novel technologies, devices and promotes technology transfer and patent licensing to the industry.

Education and Training at IMEL

Due to its unique infrastructure at a national level and the important expertise and know-how of its researchers, IMEL plays an important role in post-graduate education. It participates very actively in the following educational programmes, in collaboration with Greek universities, by providing special courses and laboratory training:

1. Post-graduate program in "Microelectronics" in collaboration with the University of Athens (for MSc and PhD degrees)
2. Master program in "Microsystems and Nanoelectronic devices" in collaboration with the National Technical University of Athens
3. Post-graduate program in "Nanosciences and Nanotechnologies" in collaboration with the University of Thessaloniki (for MSc and PhD degrees)

Laboratories and Central Fabrication Facilities at IMEL

The facilities and equipment of IMEL include a full silicon processing laboratory in a clean room area of 300 m^2 equipped with lithography (optical, e^- beam) and etching tools, thermal and chemical processing facilities, ion implantation, deposition of metals, dielectrics and poly- nanocrystalline silicon by physical and chemical processes (LPCVD, sputtering, e-gun and thermal evaporation), and process inspection equipment. Satellite laboratories include electrical and optical characterization, micromachining and packaging laboratory, resist development laboratory, electron microscopy (SEM, STM/AFM), sensor characterization and testing equipment.

The clean room area for thermal, chemical and reactive ion etching processes of the Institute has been fully upgraded to class 1000, while lithography area to class 100, in the year 2002.

A new building of the Institute has been constructed in 2006 to host the electrical, optical and structural characterization laboratories. A photograph of the building in the final stage of construction is shown in fig. 1.

Fig. 01: *View of IMEL facilities*

Management

The management of the Institute is assured by its Director, who is elected by an International Scientific Committee for 5 years, assisted by a Deputy Director and an Institute Advisory Board, elected every 2 years by the Researchers. The Director represents the Institute in the Board of management of the Centre, and is responsible for the overall functioning of the Institute.

A scientist is in charge of the processing laboratory, which is a central facility used by all scientific groups. There are also programme representatives for the 3 main R&D programmes as they appear on the organizational structure of the Institute.

An external International Scientific Advisory Committee operates at IMEL from the year 2000, which discusses with the director and the scientific staff the Institute research priorities and policy.

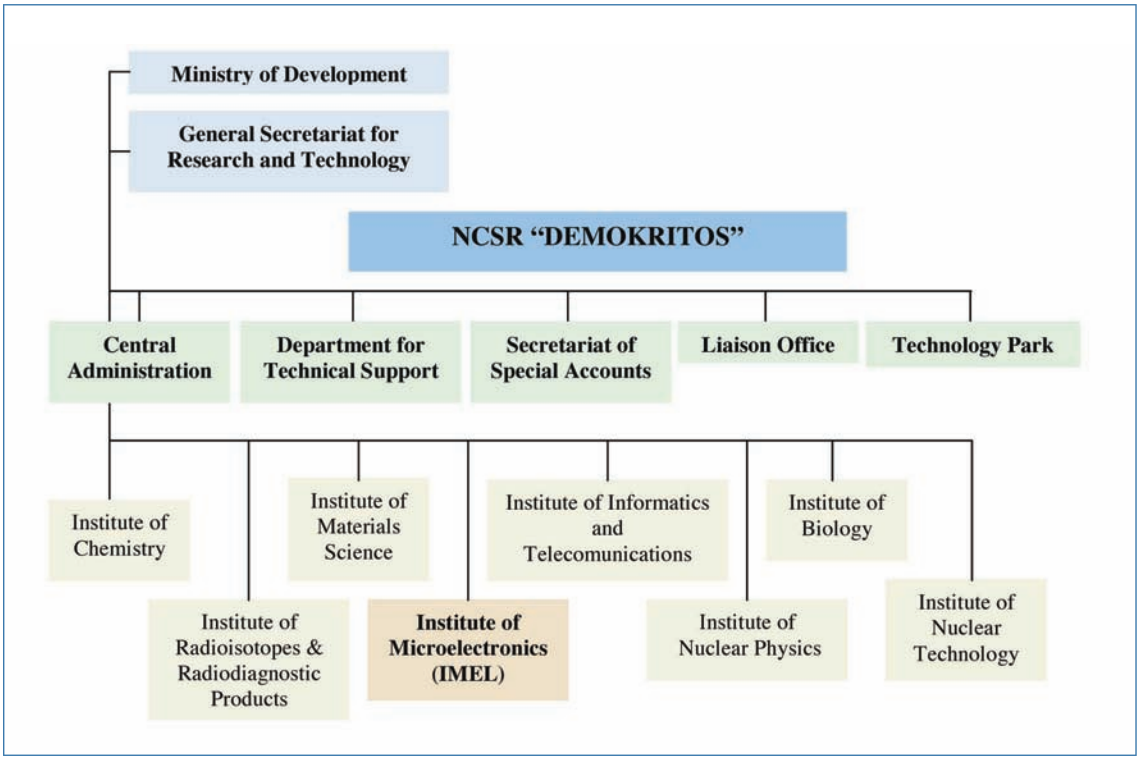
Personnel

The personnel of IMEL includes 17 key researchers and several post-doctoral scientists and PhD students. It also includes a group of technicians that operate the central fabrication facility. The names of the personnel are given in annex I.

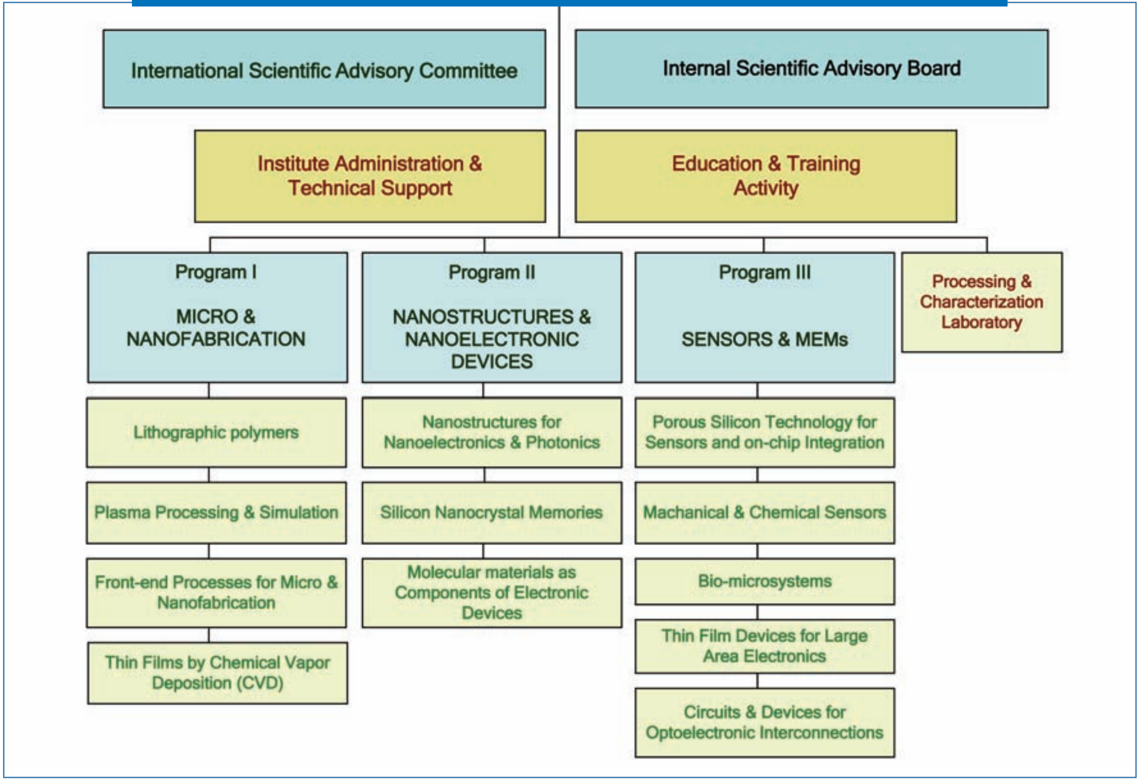
Fig. 02: *Scientific staff*

Fig. 03: *Personnel of IMEL*

ORGANIZATIONAL STRUCTURE



IMEL
Director: Dr A.G. Nassiopoulou



Research Programme I

MICRO & NANOFABRICATION

PROJECT I.1: LITHOGRAPHIC AND FUNCTIONING MOLECULAR MATERIALS

Project Leader: P. Argitis

Key Researchers: P. Argitis, I. Raptis

Other collaborating researchers: D. Davazoglou, N. Glezos, E. Gogolides, K. Misiakos, P. Normand

Post-doctoral Research Associates: M. Chatzichristidi, A. Douvas, G. Patsis, M. Vasilopoulou

Ph.D. candidates: D. Drygiannakis, D. Niakoula, P. Pavli, N. Tsikrikas

Funding

- INTEL- MoleEUV, collaboration project for EUV resists, 2003-2006
- More Moore, EU FP6 Integrated Project (IST), 2004-2006
- Nano2Life, EU FP6 Network of Excellence (NMP), 2004-2007
- PENED "CMOS-NANO" project (GSRT-PHOTRONICS funding), 2005-2008
- Greece-Hungary bilateral cooperation (HARM.PB), 2005-2006

Research orientation:

a. *Development of resist platforms for next generation lithography*

   Development of resists with potential for sub 45 nm patterning: "molecular" resists, polymer back-bone breaking, exploration of resist resolution limits

b. *Understanding and Optimization of Resist Patterning Processes: Material, Physicochemical and Process Studies*

   Priority in understanding the physicochemical phenomena encountered in ultra thin polymeric films and interfaces, and in molecular resists

c. *Materials research for new micro-nano fabrication processes*

   Investigation of materials issues for novel radiation-assisted patterning processes, including formation of 3D structures, patterning of biological systems and photochemically-induced tuning of emission properties in OLEDs

d. *Evaluation of new molecular classes as candidate components of lithographic or functioning microelectronic materials*

   Molecules which are not conventionally used in microelectronics are investigated for potential use either as components of lithographic materials or as functioning components of microelectronic devices following top-down or self-assembling processes

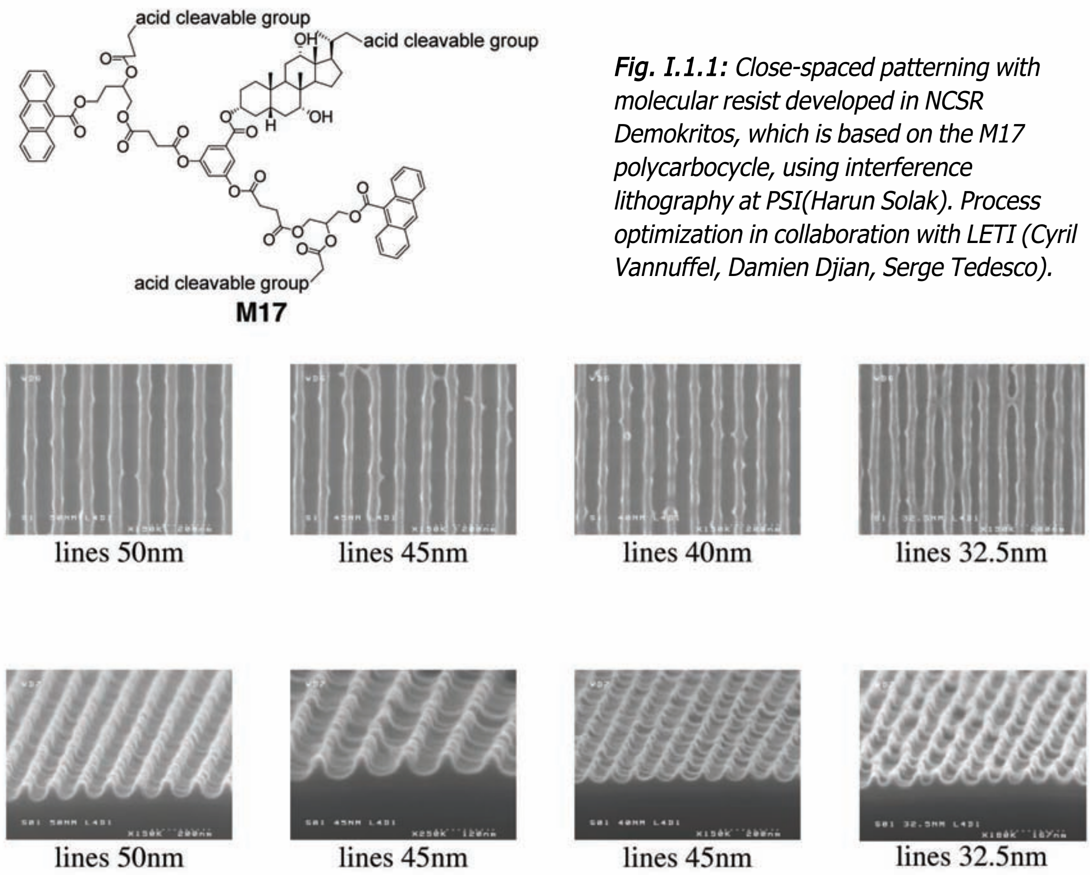
RESEARCH RESULTS

A. Development of Resists for next generation lithography

a_1 *Evaluation of polycarbocycle-based molecular resist materials for sub 50nm EUV lithograhy*

The new resist platform introduced by our group and Prof. E. Couladouros group at the Inst. of Physical Chemistry, based on the design and synthesis of new functionalized polycarbocycle molecules, was further evaluated in the context of the European project "More Moore" (2006 -) and the collaboration project with Intel.

The high resolution evaluation was mostly performed in collaboration with LETI . The EUV exposures were performed at Paul Sherrer Institute in Switzerland and e-beam exposures at LETI. Additional EUV exposures were carried out at MET (Berkeley). Close spaced sub 50 nm patterns were obtained with the resist formulation having as main component the molecule M17, after systematic process studies. The research continues towards sensitivity improvement by both material and process optimization.



lines 50nm — lines 45nm — lines 40nm — lines 32.5nm

lines 50nm — lines 45nm — lines 45nm — lines 32.5nm

Fig. I.1.1: *Close-spaced patterning with molecular resist developed in NCSR Demokritos, which is based on the M17 polycarbocycle, using interference lithography at PSI(Harun Solak). Process optimization in collaboration with LETI (Cyril Vannuffel, Damien Djian, Serge Tedesco).*

a_2 *Resists based on backbone breaking*

Backbone breaking is considered as an interesting direction for sub50 nm lithography since the Line Edge Roughness (LER) can be ultimately controlled by the size of the part of the polymer being broken and not by the polymer molecular weight. The problem is that the typical resists working by backbone breaking chemistry (e.g. PMMA) typically suffer from poor etch resistance properties since they decompose easily in the reactive plasmas used in etching. A recent direction of our research targets to overcome this problem. Promising results have been obtained so far by a polymer containing acid breakable but not photochemically active acetal bonds in the backbone.

B. Understanding and Optimization of Resist Patterning Processes: Material, Physicochemical and Process Studies

b_1 *Simulation of e-beam patterning of complex layouts*

For the fabrication of ICs in the sub-65nm nodes, the semiconductor manufacturing industry has the need to explore design for manufacturing (DFM) solutions that improve predictability, quality and yield. The complex mask data need to be verified and optimized before the fabrication process. An effective method to this direction would be to simulate the mask image and compare it with the design image for inconsistencies. With these problems in mind, a home made stochastic lithography simulator and an electron-beam exposure – pattern convolution module are integrated in order to result in a complete lithography simulator to account for high resolution layouts fabricated with electron-beam lithography. The application of stochastic modeling techniques is preferred in these length scales because all microscopic phenomena can be considered, through appropriate assignment of occurrence probabilities. In particular, the stochastic approach is applied in the simulation of resist film (polymer chains and PAG content), post-exposure bake (PEB) and development processing steps.

This combined stochastic - electron-beam simulator is applied in particular test layouts. Using this simulation approach both Critical Dimension (CD) and LER studies could be carried out on the same part of the layout, while the effects of processing conditions and photoresist materials on the design rules could be studied. In addition, LER quantification can be carried out in the length scale of each transistor in the layout and in a batch mode.

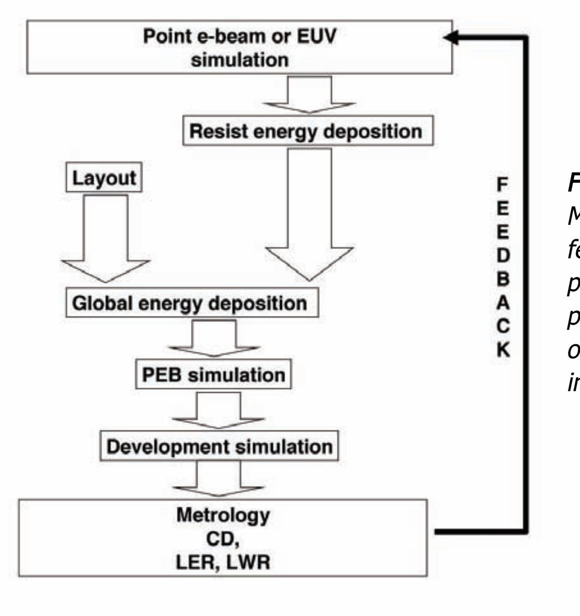


Fig. I.1.2: *Proposed simulation flowchart. Metrology on the final simulated profiles will feedback input (material/process parameters) in order to optimize the final profile prior to actual transfer of the layout on mask. LER studies can also be incorporated in this framework*

b_2 *Characterization (Physicochemical properties) of thin resist films*

The significantly reduced resist film thickness to be used for the 32 and 22nm technology nodes poses significant changes on the physicochemical properties and the dissolution properties compared to the thick films. The dissolution properties of molecular based resists were studied, for film thickness 80-100nm, for various formulation (PAG load) and processing (PAB temperature, PEB temperature, exposure dose) conditions. For this study a White Light Reflectance Spectroscopy methodology bas on interference was developed and applied. From these studies the resist composition (PAG concentration) and processing conditions (PAB, PEB conditions) for controlled dissolution were defined. At these conditions it was revealed, from high resolution EUV exposures, the lithographic performance was in the sub 35nm range.

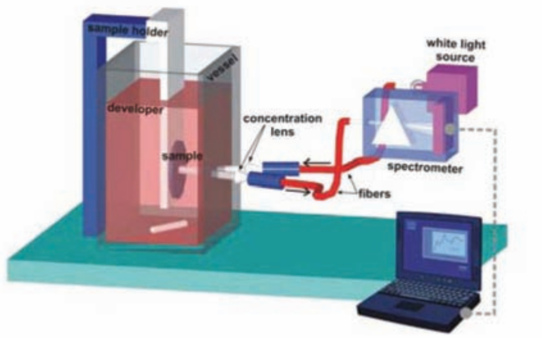


Fig. I.1.3: *Experimental set-up for evaluating dissolution properties*

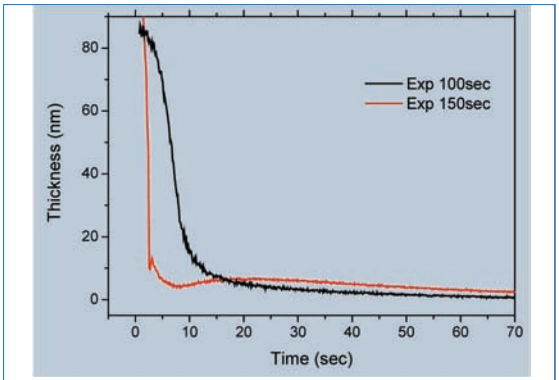


Fig. I.1.4: *Typical results demonstrating capability for monitoring dissolution processes after different exposure doses in thin (100nm or thinner) molecular resist films*

b_3 *Stochastic simulation of "molecular" and oligomer-based resists*

Stochastic Monte Carlo techniques are used with a quasi-static dissolution algorithm to simulate dissolution of polymer lattice based on the concept of critical ionization. Etching is simulated by applying an isotropic deformation on a numerically obtained line edge. Two-dimensional simulations and comparisons of the LER between films of molecular resists and resist films made of oligomers with the same molecular diameter showed that in all cases molecular resists have lower LER. Explanations of this behaviour were based on molecular architecture and the free volume distribution in the resist film. It was also found out through simulation, that the size of free volume regions is less in molecular resist than in the corresponding oligomers. In general, LER is minimum for low average degree of polymerization resists, low acid diffusion range (however, it should be appropriate for correct CD), and low secondary electron blur (SEB should be zero if possible to eliminated shot noise especially if combined with low ADP resists). Etching can be used to remove high frequency components of resist edges LER, but could deteriorate CD unacceptably in this trimming process.

C. Materials research for micro-nano structure fabrication

c_1 *Thick film patterning technologies for the fabrication of Microsystems*

Tilted structures in either thin or thick films are very interesting for various applications such as photonic crystals and microchannels. Such structures could be also used for gas/liquid handling on chips. In collaboration with the Inst. of Nuclear Research, Hungarian Academy of Sciences, a thick resist film technology based on tilted proton beam (PB) irradiation for the realization of sloped structures was developed. PB Writing is promising for the fabrication of tilted structures due to the fact that the proton beam does not broaden too much due to the interaction with matter for a large depth. In the present work, high resolution and high aspect ratio polymeric structures in SU-8 and ADEPR (aqueous developed negative resist) were resolved. The developed technology is further applied for the fabrication of long tilted microchannels clear from one end to the other with critical dimension less than 10 μm by exploiting a goniometer setup. This methodology could be applied for the implementation of "fence" structures and could be further extended to the fabrication of particular photonic structures, such as Yablonovite-type by an additional exposure to a third axis.

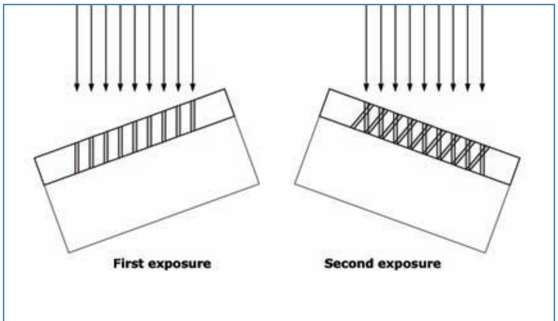


Fig. I.1.5: *Schematic representation of the tilted exposures at the goniometer setup. The sample was tilted to +20 º for the first irradiation, then -20 º for the second irradiation, and kept a well defined alignment point in the microscope view to make sure that the two irradiations will overlap*

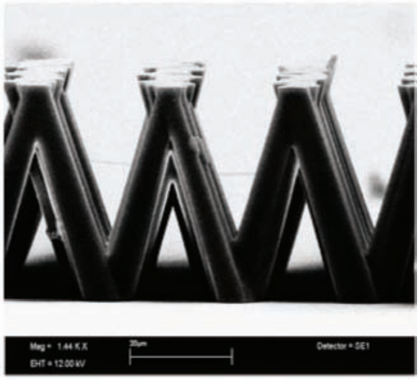


Fig. I.1.6: *Side view of the "lambda" structures of SU-8. The length of the channel is 100 μm and the wall thickness is 10 μm.*

c_2 *Investigation of interactions between organic surfaces and biological materials*

Towards the further development of resist – based biocompatible processes for the patterning of biological substances a research effort aiming at the investigations of the interactions of organic film coated substrates with biological substances has been launched. Emphasis is given on the interactions of proteins and oligonucleotides with photoresist surfaces but other organicic films, especially photochemically active polymeric films and self-assembling monolayers (SAMs) are considered.

c_3 *Photoacid induced emitting colour changes in OLEDs*

The research effort to further improve the proposed by our group patterning scheme of acid induced spectral changes in the active layer of OLEDs was conrinued. Three colour (blue-red-green) pixels have been defined (see figure). The influence of the patterning process on the efficiencies of the devices has started.

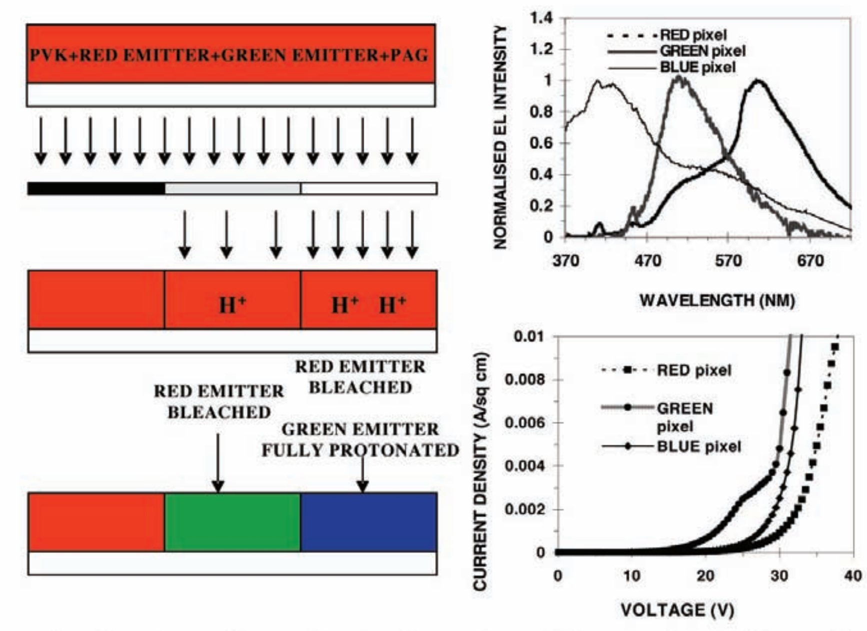


Fig. I.1.7: *Proposed patterning scheme for the formation of three colour (blue-red-green) emitting pixels in a single layer in OLEDs. Characteristic electroluminescence spectra and IVs from different colour pixels are shown.*

D. Evaluation of selected molecular classes as candidate components of lithographic or functioning microelectronic materials

d_1 Polyoxometallates

The class of Mo and W polyoxometallates, which can be considered as molecular analogs of the corresponding oxides is investigated for three different areas of applications:

a) Development of lithographic materials and nanostructuring processes with polyoxometallates as photosensitizers or as etch resistant components

b) Development of layer by layer processes for the fabrication of organized polyoxometallate single layers or multilayers that are evaluated as candidate components of memory devices in collaboration with researchers of program II (see relevant section of project II.2).

c) Development of electrochromic materials where certain polyoxometallates act as strong acids in solid state.

d_2 Functionalized polyaromatics

Polycarbocyclic molecules of the same class as the ones used as basic components of the molecular resists described above, which are based on derivatized anthracenes, are investigated as components of photonic materials with potential applications in OLEDs or in integrated sensing devices. The molecules are synthesized mainly by Dr V. Vidali and other researchers of Prof E. Couladouros' Organic Synthesis group in the Inst of Phys. Chemistry. The development of molecular glasses that are patternable and at the same time are functioning as photonic and charge transporting materials is considered as the main driving force for this research activity.

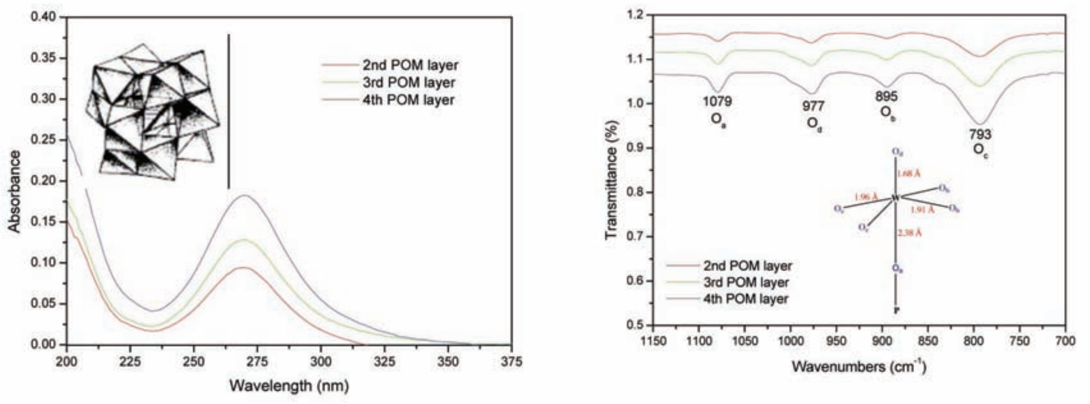


Fig. I.1.8: *UV-Vis (left) and FTIR (right) spectroscopic monitoring of layer by layer process, where the* $PW_{12}O_{40}^{3-}$ *(Keggin structure anion) is deposited using a selected diamine as the cation layer*

d_3 Macrocyclic rings

Ligand exchange reactions of metalloporphyrins were studied in collaboration with Prof. A.G. Coutsolelos of Dept. of Chemistry, Univ. of Crete. These reactions were investigated for potential application in chemical sensing devices. In particular the photochemical dechlorination of chlorinated solvents and the subsequent formation of photochemically inert Mo metalloporphyrins having chloride as one of their ligands was demonstrated. These reactions can be easily followed by UV-Vis spectroscopy. Possibilities for the use of metalloporphyrins or other macrocycles as functional elements of sensing or actuating devices are explored.

PROJECT OUTPUT in 2006

Publications in International Journals

1. Partially fluorinated, polyhedral oligomeric silsesquioxane-functionalized (meth)acrylate resists for 193 nm bilayer lithography", A.M. Douvas, F. Van Roey, M. Goethals, K.G. Papadokostaki, D. Niakoula, E. Gogolides, P. Argitis, Chemistry of Materials 18 (17), 4040-4048, 2006.
2. "Photochemically-induced ligand exchange reactions of ethoxy-oxo-molybdenum(V) tetraphenylporphyrin in chlorinated solvents", A.M. Douvas, P. Argitis, A. Maldotti and A. G. Coutsolelos, Polyhedron, 25, 3427-34, 2006.
3. "Protonic methacrylate polymeric electrolytes for all-solid-state WO3-based electrochromic displays", M. Vasilopoulou, I. Raptis, P Argitis, G. Aspiotis and D Davazoglou, Microelectron Eng., 83, 1414-1417, 2006.
4. "Electrical characterization of molecular monolayers containing tungsten polyoxometalates", Nikos Glezos, Antonios M. Douvas, Panagiotis Argitis, Frank Saurenbach, Juergen Chrost and Christos Livitsanos, Microelectronic Engineering, 83, 1757-1760, 2006.
5. "Layer-by-layer UV micromachining methodology of epoxy resist embedded microchannels", M. Kitsara, M. Chatzichristidi, D. Niakoula, D. Goustouridis, K. Beltsios, P. Argitis and I. Raptis, Microelectronic Engineering, 83, 1298-1301, 2006.
6. "Electron beam lithography simulation for the fabrication of EUV masks", G.P.Patsis, N.Tsikrikas, I.Raptis, N.Glezos Microelectron. Eng. 83 1148(2006)

7. "Off line metrology on SEM images using gray scale morphology", E.N.Zois, I.Raptis, V. Anastassopoulos Microchim. Acta 155 323(2006)
8. "Pattern guided structure formation in polymer films of asymmetric blends", J.Raczkowska, A.Bernasik, A.Budkowski, P.Cyganik, J.Rysz, I.Raptis, P.Czuba Surf. Sci. 600 1004(2006)
9. "Multi-wavelength interferometry and competing optical methods for the thermal probing of thin polymeric films", N.Vourdas, G.Karadimos, D.Goustouridis, E.Gogolides, A.G.Boudouvis, J.-H.Tortai, K.Beltsios, I.Raptis J. Appl. Polym. Sci. 102 4764(2006)
10. "Thickness-dependent glass transition temperature of thin resist films for high resolution lithography", S.Marceau, J.-H.Tortai, J.Tillier, N.Vourdas, E.Gogolides, I.Raptis, K.Beltsios, K.van Werden, Microelectron. Eng. 83 1073(2006)
11. "Nano-scale spatial control over surface morphology of biocompatible fluoropolymers at 157 nm", E. Sarantopoulou, Z. Kollia, A. C. Cefalas, A.M. Douvas, M. Chatzichristidi, P. Argitis, S. Kobe, Materials Science and Engineering C, in press, available online 17 November 2006.
12. "A biomolecule friendly photolithographic process for fabrication of protein microarrays on polymeric films coated on silicon chips", P.S. Petrou, M. Chatzichristidi, A. M. Douvas, P. Argitis, K. Misiakos and S.E. Kakabakos, Biosensors and Bioelectronics, in press, available online 5 October 2006.

Publications in International Conference Proceedings

1. "Stochastic simulation studies for the dissolution of molecular resists", D. Drygiannakis, G. P. Patsis, I. Raptis, D. Niakoula, V. Vidali, E. Couladouros, P. Argitis, E. Gogolides, Abstract book, 32nd International Conference on Micro- and Nano- Engineering, MNE 06, September 2006, Barcelona Spain, 3rd poster award.
2. "Photolithographic Process, Based on High Contrast Acrylate Photoresist, for Multi Protein Patterning", M. Chatzichristidi, P.S. Petrou, A. Douvas, C.D. Diakoumakos, I. Raptis, K. Misiakos, S.E. Kakabakos, P. Argitis, Abstract book, MRS 2006 Fall Meeting, Boston, USA, November 27-December 1, 2006, p.96.
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2. A. M. Douvas, K. G. Papadokostaki, K. Yannakopoulou, D. Niakoula, E. Gogolides, P. Argitis, Polyhedral-Oligomeric-Silsesquioxane (POSS) containing Resists for 193 nm Bilayer Lithography: The Effect of Partial Fluorination on the Lithographic Behaviour, Book of Abstracts, 6th Hellenic Conference on Polymers, Patras, 3-5 November 2006, p. 120

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Final Report on Intel funded project
"MolEUV: Novel Molecules for EUV Lithography - A new approach to photoresist design, coupled with fractal description and molecular simulation of roughness", August 2006

PhD thesis

Dimitra Niakoula, Chemist, Thesis title: Polymeric materials and processes for lithography in thin films, Department of Chemistry, Polymer Science and Applications Graduate Program, University of Athens, Thesis Defense: November 2006

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1. P. Argitis, E. Gogolides, D. Niakoula, V. Vidali, E. Couladouros, R. Gautan, "Molecular resists based on polycarbocycle derivatives", Greek Patent (OBI) appl. 20050100472/ 16-9-2005, International Patent Application PCT/GR06/000050 19/9/2006
2. P. Argitis, G. Pistolis, M. Vasilopoulou, Tuning the emitting color of single layer, patterned full color Organic Light Emitting Diodes, Greek Patent (OBI) appl. No 20060100359, 19 June 2006

PROJECT I.2: LITHOGRAPHY and PLASMA PROCESSES

Project Leader: E. Gogolides

Key Researchers: E. Gogolides, A. Tserepi

Collaborating Researchers: K. Misiakos, I. Raptis, P. Argitis, C.Tsamis, S. Chatzandroulis

Post-doctorals Researchers: G. Patsis, V. Constantoudis, G. Kokkoris

PhD candidates: P. Bayiati, N. Vourdas, M. Vlachopoulou, G. Boulousis, K. Tsougeni, A. Malenou

Projects Running:

- EU IST IP More Moore, Contract No 507754, 1/1/2004-31/3/2007
- IEU NMP NoE Nano2Life, Contract No 500057, 1/2/2004-31/1/2008
- Contract with the company INTEL- MoleEUV, 1/5/2003-30/4/2006
- EU NMP2 STREP Nanoplasma, Contract No 016424, 1/4/2006-31/3/2009
- GSRT, PENED 03 ED 202, 1/12/2005-31/11/2008

Objectives:

Our work in nanopatterning focuses both on lithography and etching / processing: For lithography we focused on predicting the process and material effects on Line Edge Roughness (LER) and on nano transistor operation. We have proven for the first time that not only the sigma value of LER, but also the correlation length greatly impacts the device operation. Thus, small diffusion lengths during baking processes, and molecular photoresists are recommended. A demo of our LER measurement software is online on our site, while our molecular stochastic lithography simulator is steadily progressing.

For plasma process nanopatterning / nanotexturing we are studying nanotexturing of Si, and polymers. Our results for PDMS, and PMMA polymers have shown impressive high aspect ratio plasma induced nanotexture, and creation of superhydrophobic surfaces within 1 min of plasma processing. A PCT patent was filed, and two publications in Nanotechnology have appeared. Nanotexturing is being studied both by continuum and Monte Carlo models developed in our group. The continuum approach tries bring our level set based profile simulation algorithms to the nanoscale. Our level set based profile simulator will be available as demo software on our site within 2007.

This year a new plasma based nanotechnology project was initiated. The NANOPLASMA project funded by EU brings together plasma equipment industry, research and academia to design a feedback controlled next generation plasma etcher, capable of controlling the etch rate, profile evolution, and nanotexture / nanoroughness formation. The role of our group is to provide fast zero dimensional gas and surface kinetics modules, and to study the nanotexturing-nanoroughness formation.

Microfluidics fabrication and actuation has consumed significant effort. We are proposing an alternative technology for microfluidics patterned on polymeric substrates using plasma etching and plasma functionalisation. First results have been achieved on PMMA. Within less than half an hour processing in our ICP etcher we fabricate rectangular 20micron deep channels in polymers such as PMMA, and we are evaluating them for capillary electrophoresis. First results are available this year and demonstrate the viability of this mass production amenable technology.

RESEARCH RESULTS

A. Nanopatterning: Metrology, simulation and impact on nano-transistor performance of Line Edge Roughness (LER, LWR)

a_1 *Effect of LER on nano transistor performance: a metrological point of view*

V. Constantoudis, G. Patsis, E. Gogolides

From the metrological analysis of LER in previous years, we have concluded that the characterization of LER demands the determination of three parameters : a) the r.m.s. value R_q measured at infinite line length, b) the correlation length ξ and c) the roughness exponent α. (see Demo Software, http://www.imel.demokritos.gr/software.html). This year, the aim has been to determine the impact of these LWR parameters on transistor electrical operation and to connect material and process parameters with these effects. To this end, we have examined first the impact of LWR on threshold voltage shifts by using model lines with fractal self-affine characteristics for the simulation of transistor gate morphology. It has been found that for resist lines or transistor gates with constant sigma LWR σ_{LWR}, the decrease of spatial LWR parameters (correlation length ξ and roughness exponent α) leads to smaller deviations from the designed electrical transistor performance (see figure I.2.1). Second, the effects of photoresist polymer length and acid diffusion length on LWR parameters and transistor performance are investigated. Through the application of the simulator of the lithographic process described in the next sub-task, it has been shown that photoresists with small polymer chains and small acid diffusion lengths form lines with low LWR parameters (r.m.s. LWR σ_{LWR}, ξ , α) and thus lead to transistors with more reliable electrical performance. We also found that CD variation has more drastic effects on threshold voltage shift than LWR.

a_2 *Simulation of lithography for LER reduction and design layout corrections*

G. Patsis, G. Kokkoris, V. Constantoudis, D. Drigiannakis, I. Raptis, E. Gogolides

We try to understand how lithographic material and processing, affect LER, and device operation. Stochastic Monte Carlo techniques are used with a quasi-static dissolution algorithm to simulate dissolution of polymer lattice based on the concept of critical ionization. Etching is simulated applying an isotropic deformation on a numerically obtained line edge. Two-dimensional simulations have shown that molecular resists have lower LER (see Project I.1 molecular resists) compared to conventional low MW resists. LER is also minimized with low acid diffusion range, and low secondary electron blur. Etching can be used to remove high frequency components of resist edges LER. The simulation was extended all the way to device operation, as discussed in task (a) above. Combined CD and LER simulation on critical places of a design in terms of exposure, material and processes are important aspects for the quality of the devices. The current methodology could deliver CD and LER metrology on a realistic layout, rather than model resist lines. Thus, it becomes possible to perform design optimization in terms of both CD and LER, while today usually only CD is considered (fig. I.2.2)

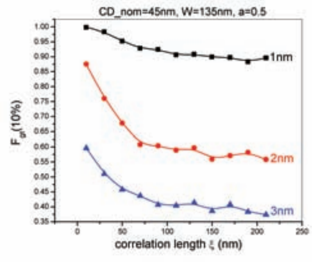


Fig. I.2.1: *Fraction of reliable transistors (yield)* F_{gt} *vs correlation length for LER 1sigma=1,2 and 3nm. Notice the dramatic effect on yield of both sigma value and correlation length.*

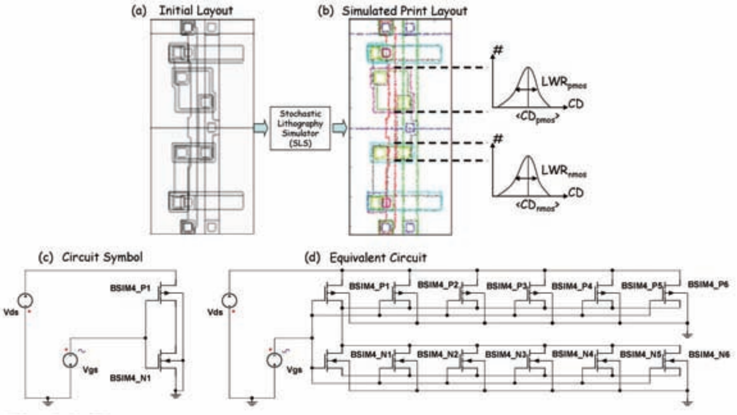


Fig. I.2.2: *(a) Drawn layout of CMOS inverter. (b). Simulated layout with the proposed methodology, and determination of the transistor gate length distributions. (c) Standard device level description of the the CMOS inverter. (d). Proposed CMOS inverter description where the sub-devices have properties determined by the gate length distributions determined in (b).*

B. Microfluidics fabrication and actuation using plasma processes

b_1 Plasma etching for fabrication of PMMA Microfluidic devices

N. Vourdas, K. Kontakis, K. Tsougeni, E. Gogolides

The fabrication of microfluidic devices with features of 10-1000 μm size are of great importance in many fields of analytical science, where a small quantity of sample is available, enhanced resolution and sensitivity in separation is needed and increased functional integration is desired (medical, chemical and biochemical analysis, microchemistry etc).

We propose an alternative method for fabrication of microfluidic devices based on direct O_2 plasma etching of polymers -PMMA in particular- using photosensitive Si-containing polymeric mask (poly-dimethylsiloxane-PDMS). Surface roughness characteristics are controlled by means of plasma parameter tuning. Electroosmotic flow (EOF) measurements are conducted to validate the functionality of our devices. Electrokinetic parameters found to be greatly influenced from the time after the fabrication of the device (recovery phenomena).

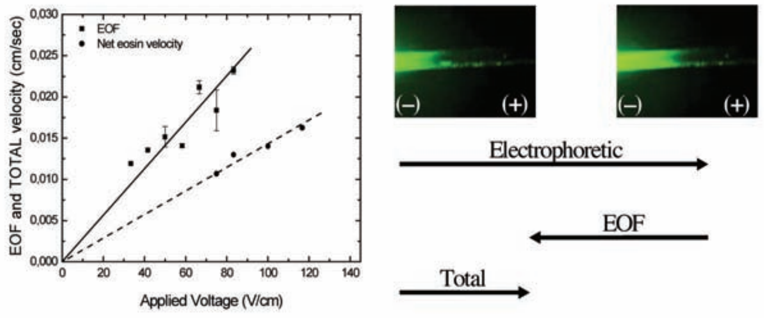


Fig. I.2.3: *velocities against applied voltage (Right) Snapshot from the fluorescence microscope monitoring the negatively charged Eosin transport in an aged device. EOF mobility is lower than the electrophoretic, causing the Eosin to move towards the anode.*

b_2 *Fabrication technologies for microfluidic devices based on soft lithography and novel bonding techniques*

M. Vlachopoulou, A. Malenou, A. Tserepi, K. Misiakos

We have adopted the process of replica molding (soft lithography) based on the lithography of SU(8) (mold fabrication) for the rapid prototyping of PDMS-based microfluidic devices. Open PDMS channels have been fabricated by this technique and are sealed using O_2 plasma activation for bonding PDMS channels on PDMS or glass, as shown in Fig.I.2.4 below. We have developed a novel process using a combination of O_2 plasma activation and surface functionalization with APTES for irreversibly bonding channels fabricated in PDMS on a PMMA cover plate, as shown in Fig.I.2.5, or bonding PDMS with Polysterene, and SU8. This novel process is also useful for irreversible bonding of PMMA with PMMA, using a thin flat piece of PDMS as intermediate layer, as well as for improving the adhesion of a PDMS spin-coated film on a PMMA sheet. The same process can be used for the irreversible bonding of PMMA with Si and glass, without using a flexible intermediate layer; it is thus suitable for a wide range of materials. A variety of devices have been fabricated with the above process. The closed channels shown in Fig. I.2.4 are appropriate for capillary electrophoresis experiments, while in Fig. I.2.6 a PDMS-based gas chromatography microcolumn is shown, which combined with a gas sensor enhances the resolution of gas detection on the sensor.

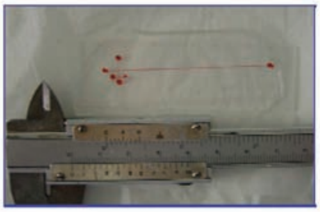


Fig. I.2.4: *75 μm deep PDMS microchannel fabricated with soft lithography & irreversibly bonded on a glass substrate, appropriate for capillary electrophoresis experiments.*

Fig. I.2.5: *100 μm deep PDMS microchannels fabricated with soft lithography and irreversibly bonded on a PMMA plate.*

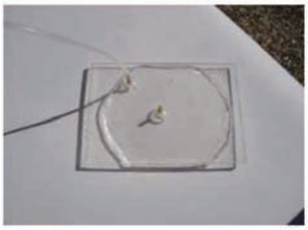


Fig. I.2.6: *Chromatography microcolumn fabricated in PDMS with soft lithography and irreversibly bonded on spin-coated PDMS spin-film, well-adhered on a PMMA plate used for mechanical support of the fluidic interconnects.*

b_3 *Plasma deposited films for electrowetting-based actuation in microfluidics*

P. Bayiati, A. Tserepi, K. Misiakos

Our work in the use of plasma-deposited fluorocarbon films started a few years back for application in electrowetting-based actuation in microfluidics. Droplet-based microfluidics, or "digital" microfluidics, is a fascinating emerging field, promising to offer an enabling technology for manipulating micro- to pico-liter sample volumes, and an expanding spectrum of potential applications in drug discovery, diagnostics and health care. Although several actuation methods have been employed so far, electrowetting on dielectric (EWOD) seems to be very promising. In the present work, optimized fluorocarbon films were deposited in C_4F_8 plasma on Si_3N_4 (for improvement of dielectric properties) and electrowetting experiments were conducted using protein solutions. Such hydrophobic films show high contact angle modulation upon voltage application, good contact angle reversibility upon voltage removal and negligible protein adsorption, all independent of pH and concentration of protein solutions, and applied voltage polarity. Thus, plasma deposited fluorocarbon films, have certain advantages compared to spin-coated commercial films (thickness homogeneity across the covered surface and good adhesion to the substrate) could replace the latter materials used routinely in electrowetting-based applications. Ultimately, fluid transport was demonstrated on an open microfluidic device fabricated using plasma deposited hydrophobic fluorocarbon films of optimized properties.

C. Plasma nanostructuring-nanotexturing of polymers and silicon

c_1 Design and Control of Surface Wetting properties of PDMS by plasma processing and casting solvents

M. Vlachopoulou, A. Tserepi, K. Beltsios, E. Gogolides

Polydimethyl-siloxane (PDMS) is a material widely used as a structural material of microfluidic devices. Control of the surface topography and the resulting wetting properties has been achieved using SF_6 plasma treatment. The dependence of PDMS surface topography on processing parameters is investigated and specifically on the casting solvents used for the preparation of PDMS samples. For the first time is demonstrated that chain packing arrangement can affect the topography of PDMS under plasma-based nanostructuring of its surface and controlled variation of surface roughness and column spacing is achieved. In Fig.I.2.7 the monotonic dependence of the PDMS etch rate on the solvent quality is presented and the effect of relaxation of polymeric chains is shown as samples are refrigerated at -20°C, while in Fig.I.2.7.b the height of nano-columns seems to be monotonically dependent on the solvent quality, for samples with fixed film thickness. Consequently, the quality of casting solvents is found to affect in a controlled way the PDMS nanostructuring.

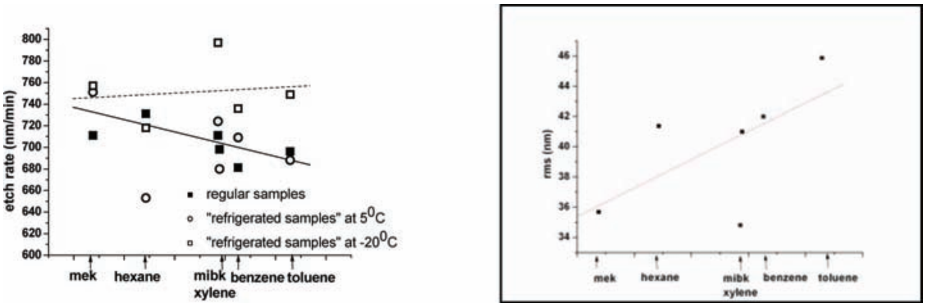


Fig. I.2.7: *Monotonic dependence of the PDMS etch rate and of the height of nanocolumns created in SF_6 plasma on the casting solvent quality.*

c_2 Design and Control of Surface Wetting properties of PMMA by plasma processing

N. Vourdas, A. Tserepi, E. Gogolides

Wettability control of polymers is of great importance in many industrial and scientific areas; from manufacturing of water repellent surfaces to droplet frictionless motion in microfluidics, and biocompatibility tuning. Wetting or repellent behavior is governed by both surface chemistry and topography. In particular, super-hydrophobicity (SH) is attained by combining low surface energy coatings and high-aspect-ratio (HAR) geometrical characteristics. In this study we proposed a novel, simple, generic and fast technique to fabricate stable SH, yet transparent poly(methyl methacrylate) (PMMA) surfaces by means of high-density plasma etching and deposition. Similar method has been already utilized to produce SH poly(dimethyl methacrylate) (PDMS) by our group (see above) .

Our Inductively Coupled source is used to generate cold plasma within a low-pressure reactor which is used to treat the PMMA surfaces. First oxygen based plasma is applied to etch the surface and create surface roughness. The time of the process may differ from 1 min to several min depending on the roughness amplitude and on the degree of transparency desired. After this first step the gas chemistry is altered into a fluorocarbon one which leads to a Teflon-like deposition and controlling thus the surface chemistry. Following this process SH surfaces are produced, which attain water contact angle: ~150°, with low hysteresis: <10°.

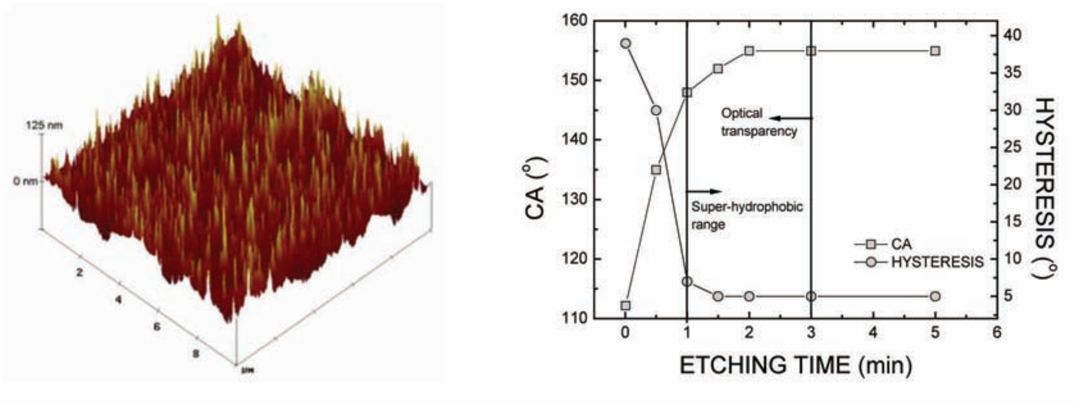


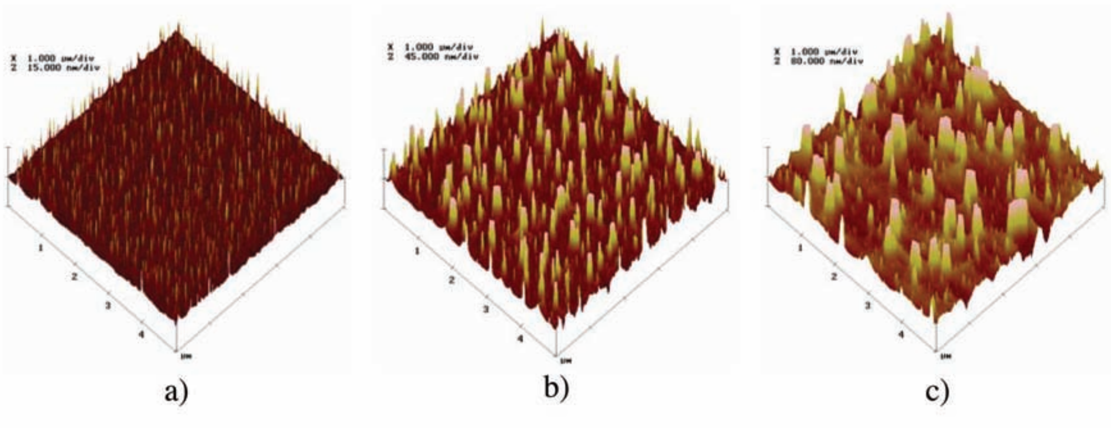
Fig. I.2.8: *AFM image of the 1 min Oxygen plasma treated PMMA surface. (right) Contact angle (CA) and CA-hysteresis of plasma treated PMMA surfaces vs. Oxygen plasma treatment time (after Teflon coating).*

c_3 *Dual scale Nanoroughness formation on silicon surfaces using SF6 plasma etching*

G. Boulousis, G. Kokkoris, V. Constantoudis, E. Gogolides

The primary target of this work is the control and understanding of roughness, which is created in a silicon substrate after fluorine based plasma-etching process, targeting smooth Microsystems fabrication or deep trench isolation etching. Roughness evolution is studied as as a function of etch-time, temperature, wall reactor condition and intentionally introducing depositing gases in the plasma.

Roughness is studied with AFM and scaling analysis of the AFM image is done. We find that roughness always increased with time, and the fraction rms/etch-depth remains below 0.1 %. It is observed that the etched silicon surfaces show dual scale topography namely an underlying nanoroughness with superimposed nanoneedles (nanograss, nanopillars). Scaling Analysis of the AFM images using Height-Height correlation functions and Fast Fourier Transforms (software developed in house) provide the periodicity of surface λ (related to the period of underlying nanoroughness structure), the correlation length ξ (related to the nanoneedle diameter) and the component of roughness of each surface. It is found that all these components increase linearly with time resulting in coarser and larger pillars and valleys as time progresses.



a) b) c)

Fig. I.2.9: *AFM images of SF$_6$ plasma etched silicon substrates for a) 1min with rms$_{u.s.}$=0.9549 nm, rms$_{needles}$=0.3010 nm, etch depth=5.4 µm, rms/E.D.=2.08 x 10^{-4}, peak to peak=22.169 nm, b) 4 min with rms$_{u.s.}$=6.8414 nm, rms$_{needles}$=3.4354 nm, etch depth=21.2 µm, rms/E.D.=4.31 x 10^{-4}, peak to peak=113.97 nm, c), 8 min with rms$_{u.s.}$=14.4736 nm rms$_{needles}$=9.2828 nm, etch depth=38.7 µm, rms/E.D.=5.37 x 10^{-4}, peak to peak=278.80 nm.*

D. Simulation of micro and nano-structuring evolution from plasma processes

d_1 *Nanoscale topography evolution using continuum models*

G. Kokkoris, P. Xydi, E. Gogolides, A. Tserepi

A robust framework for the simulation of topography evolution of rough curves (2d) and surfaces (3d) has been developed. It is based on the level set method and is applied in the simulation of profile evolution in the nano-scale. Rough surfaces (and curves) which usually result from nanofabrication processes, both periodic and self-affine, evolve under plasma etching (low sticking coefficient conditions) or under wet etching. The evolution of root mean square (rms) roughness, correlation length (ξ) and roughness exponent (α) is studied. The surface roughness is shown to decrease under etching through a cusp formation mechanism. The effect of etching mechanisms (isotopic, anisotropic) on the topography evolution is investigated. Comparison with Monte Carlo Simulation (see below) is done.

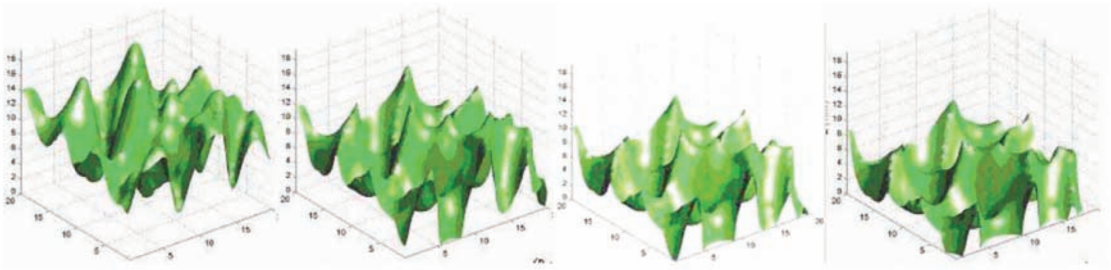


Fig. I.2.10: *The evolution of a rough surface under plasma etching (50% isotropic + 50% anisotropic)*

d_2 Stochastic simulation of roughness evolution of homogeneous and composite materials during plasma etching

A kinetic Monte Carlo simulator of the roughness formation on surfaces of films during their plasma etching has been developed. This simulator can consider etching by neutral etchants and ions. It can also include the simultaneous deposition of etch resistant particles (inhibitors). Multiple reemissions of neutrals and/or inhibitors are taken into account. It has been found that the combination of inhibitor deposition and neutral reemission may lead to the formation of surface roughness with dual scale features in agreement with experimental results.

We also examined roughness formation on composite materials. In the case of composite material sputtering, it has been shown that even tiny correlations in the phase material distributions increase significantly the growth rate of surface roughness. Whereas, in chemical etching, the roughness growth is slower and depends on the etch selectivity of the two phases in the film as well as their relative volume fractions. Also, an interesting transition from anomalous to normal scaling behavior has been observed in surface roughness as etching proceeds for large values of selectivity.

Finally the roughness reduction of initially rough surfaces of homogeneous films induced by chemical etching has been simulated. It has been found that surfaces with lower correlation length and wavelength "lose" their roughness faster than those with larger spatial features. Further, the rate of roughness reduction decreases with the fractal dimension of initial surface. Comparing with the continuum simulation results of wet etching (see above), we reached the conclusion that wet etching leads to faster reduction of periodic surfaces whereas the opposite is true for fractal self-affine surfaces.

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K., van Werden, K., Microelectronic Engineering 83 (4-9 SPEC. ISS.), pp. 1073-1077, 2006

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2. "Super-hydrophobic transparent polymer surfaces fabricated by plasma etching and deposition", N. Vourdas, M.-E. Vlachopoulou A. Tserepi, E. Gogolides, 53rd AVS Symposium, San Francisco, PS2-ThM7, p. 149, November 12-17, 2006
3. "Electroweting-based fluidic transport on hydrophobic fluorocarbon films deposited in plasma", P. Bayiati, A. Tserepi, P. S. Petrou, K. Misiakos, S. E. Kakabakos, E. Gogolides, 5th International Electrowetting Meeting, University of Rochester, New York, USA, p. 15, 31 May- 2 June 2006
4. "Biofluid transport on hydrophobic plasma deposited fluorocarbon films", P. Bayiati, A. Tserepi, P. S. Petrou, S. E. Kakabakos, K. Misiakos, E. Gogolides, C. Cardinaud, 32nd International Conference on Micro- and Nano-Engineering, Barcelona, p. 113, Spain, 17-20 September 2006
5. "Photosensitive Poly-dimethylsiloxane (PDMS) materials for Microfluidic Applications", K. Tsougeni, A. Tserepi, E. Gogolides, 32nd International conference of Micro- and Nano- Engineering, Barcelona Spain, p. 797, Sept. 2006
6. "A novel process for irreversible bonding of PDMS and PMMA substrates", M.E. Vlachopoulou, A. Tserepi, K. Misiakos, 32nd International Micro and Nanoengineering, Sept. 2006, Barcelona Spain, p. 421, Sept. 2006
7. "Nanostructuring of PDMS surfaces: Dependence on casting solvents", M-E. Vlachopoulou, A. Tserepi, K. Beltsios, G. Boulousis, E. Gogolides, 32nd International Micro and Nanoengineering, Barcelona Spain, p. 635, Sept. 2006
8. "Line-width roughness analysis of EUV resists after development in homogenous CO2 solutions using CO2 compatible salts (CCS) by a three-parameter model", Constantoudis, V., Gogolides, E., Patsis, G.P., Wagner, M., DeYoung, J., Harbinson, C., SPIE - The International Society for Optical Engineering, 6153 II, art. no. 61533W, 2006
9. "Integrated simulation of Line-Edge Roughness (LER) effects on Sub-65 nm transistor operation: From lithography simulation, to LER metrology, to device operation", Patsis, G.P., Constantoudis,

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10. "Monolithic silicon optoelectronic devices for protein and DNA detection", Misiakos, K., Petrou, P., Kakabakos, S.E., Vlachopoulou, M., Tserepi, A., Gogolides, E., Proceedings of SPIE - The International Society for Optical Engineering, 6125, art. no. 61250W, 2006

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1. "Anomalous scaling behaviour in the kinetic roughening of etched surfaces", V. Constantoudis, P. Xydi, G. Kokkoris, H. Zakka, P. Angelikopoulos, G. Boulousis and Evangelos Gogolides, Dynamic Days Conference, Crete, Greece, September 27-29 2006
2. "Effects of Lithography Nonuniformity on Device Electrical Behavior. Simple Stochastic Modeling of Material and Process Effect on Device Performance", G. P. Patsis, V. Constantoudis, and E. Gogolides, Poster 11th International Conference on Computational Electronics IWCE: 25-27 May 2006, Technical University of Wien Austria
3. "Fabrication of super-hydrophobic, water repellent pmma surfaces by plasma processes", N. Vourdas, A. Tserepi, E. Gogolides, 6th Panhellenic Conf. on Polymers, ELEP, Patras, Hellas, 3-5.11.06
4. "Thermal characterization of thin supported polymer films via interferometry and spectroscopic ellipsometry", N. Vourdas, G. Karadimos, D. Goustouridis, E. Gogolides, A.G. Boudouvis, K. Beltsios, I. Raptis, 6th Panhellenic Conference on Polymers, ELEP, Patras, Hellas, 3-5.11.2006
5. "A novel microfabrication technology for plastic sensors formation", K. Tsougeni, G. Kaltsas, A. Petropoulos, P. Asimakopoulos, D. N. Pagonis, T. Speliotis, E. Gogolides, A.G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Material Science. Patras 24-27 September 2006
6. "Control of Poly(dimethylsiloxane) surface wetting properties from very hydrophilic to super-hydrophobic by tuning surface topography in O_2 plasmas", K. Tsougeni, A. Tserepi, G. Boulousis, E. Gogolides, 6th Panhellenic Polymer Conference, Patras 3-5 November 2006
7. "Surface Silylation of Epoxidized Polymers for Micromachining Applications", D. Kontziampasis, K. Beltsios, E. Tegou, E. Gogolides, 6th Panhellenic Polymer Conference, Patras 3-5 November 2006
8. "Stochastic modeling of roughness formation during etching of composite materials", E. Zakka, V. Constantoudis, E. Gogolides, XXII Panhellenic Conference of Solid State Physics and Material Science. Patras 24-27 September 2006
9. "Polydimethyl Siloxane Microfluidic chip for gas chromatographic separations", A. Malainou, ME Vlahopoulou, A. Tserepi, S. Chatzandroulis, XXII Panhellenic Conference of Solid State Physics and Material Science. Patras 24-27 September 2006
10. "Metallization using an epoxy resist and lift-off process for microsystem fabrication", D. Kontziampasis, E. Gogolides, XXII Panhellenic Conference of Solid State Physics and Material Science, Patras, 2006

M. Sc theses

1. "Modeling of the gas phase of oxygen plasma discharges with global zero dimensional models", P. Geka, NTUA 2006
2. "Plasma etching of composite materials: Stochastic simulation of roughness formation", E. Zakka, UOA 2006

3. "Simulation of etching using the narrow band level set method", P. Zydi, UOA 2006
4. "Monte-Carlo roughening during thin film plasma etching", P. Aggelikopoulos, NTUA 2006
5. "Polydimethyl Siloxane Microfluidic chip for gas chromatographic separations", A. Malainu, NTUA 2006

New Patent Applications

1. "Molecular resists based on functionalized polycarbocycles", P. Argitis, E. Gogolides, D. Niakoula, V. P. Vidali, E. Couladouros, D. Gautan, PCTGR06/000050, 18/9/06 (Greek priority in OBI 20050100472, 16/09/2005)
2. "Method for the fabrication of surfaces of high surface area ratio on polymer/ plastic substrates", A. Tserepi, E. Gogolides, K. Misiakos, N. Vourdas, M. Vlahopoulou, CT/GR2006/000011, 8/03/06 (Greek Priority in OBI 20050100473, 16/09/2005)
3. "Bonding method", K. Misiakos, A. Tserepi, M-E. Vlachopoulou, Application in OBI (Greek Priority 20060100518/15.9.2006)

PROJECT I.3: FRONT-END PROCESSES

Project Leader: C. Tsamis

Collaborating researchers: P. Normand, V. Ioannou–Sougleridis

Post-doctoral Scientist: D. Skarlatos

PhD candidates: A. Chroneos, N. Ioannou, N. Kelaidis

Funding:

- GSRT-PENED-03ED496, "Dopant diffusion and activation in Group-IV semiconductors (Strained Silicon and Germanium) for novel nanoelectronic devices" (C. Tsamis)
- GSRT-NON-EU-204, "Process-induced strain modification in strained silicon layers and influence on device performance" (C. Tsamis)

Objectives:

- Study of dopant diffusion/activation and point/extended defect kinetics in Group-IV semiconductors (Silicon, Strained Silicon, Germanium) for CMOS applications
- Thermal processes for ultra-thin gate dielectrics (oxides, oxynitrides) in Group-IV semiconductors for CMOS applications
- Process optimization for Nanodevices (Fabrication, Electrical Characterization)
- Continuum and atomistic simulation of processes and devices

RESEARCH RESULTS

A. Dopant diffusion and defects in silicon

a_1 Modelling of low energy – high dose Arsenic diffusion

D. Skarlatos and C. Tsamis

In this work we are developing a macroscopic model in order to simulate arsenic diffusion after low-energy, high-dose implantation and subsequent annealing. Low energy implantation suppresses TED phenomenon due to extended defects dissolution in the presence of the free silicon surface. Under these implantation conditions arsenic enhanced diffusion takes place via bulk interstitial generation due to arsenic clustering. Theoretical studies and experimental evidence indicate that As clusters form around a vacancy with the consequent injection of silicon interstitials. The most probable As cluster configuration consists of four arsenic atoms surrounding a vacancy.

The approach consisted in simulating the diffusion both of arsenic, implanted with low energy and high dose, and of boron in buried δ-doped layers that exist below the implanted surface after RTA annealing at 900ºC. Secondary ion mass spectrometry (SIMS) was used to monitor arsenic and boron profiles. Simulations have been performed using Synopsys-Taurus process simulator and by solving the arsenic diffusion equation with an additional interstitial generation term, describing the interstitial generation at high arsenic concentrations due to arsenic clustering. The generation term is expressed as the difference between the chemical (total) and active (non-clustered) arsenic profiles divided by the number of arsenic atoms participating to a cluster formation. Better agreement can be achieved for both profiles, compared to the standard model (Fig. I.3.1)

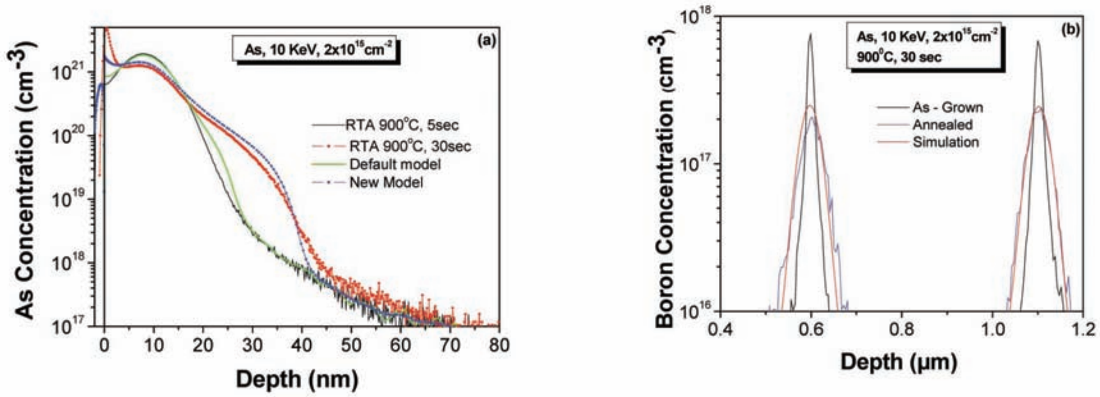


Fig. I.3.1: *Experimental and simulated arsenic (a) and boron (b) profiles during diffusion at 900^{0}C for 30 sec. Better agreement is obtained with the new model compared with the standard one.*

B. Ultra-thin oxide growth in Strained Silicon

N. Kelaidis, D.Skarlatos, V. Ioannou–Sougleridis and C. Tsamis

Integrated circuits industry has entered the nanoscale era exploring alternate high carrier mobility substrates, which enable the development of devices of enhanced performance compared to standard silicon technology. One of the most important materials is Strained Silicon (s-Si). The study of oxide formation on Strained Silicon grown Si_xGe_{1-x} substrates is of particular interest, since excess thermal processing can relax the s-Si epilayer and induce Ge diffusion towards the surface, which will deteriorate the integrity of the s-Si/SiGe heterojunction, the s-Si overlayer and the s-Si/SiO_2 interface. A method of improving the oxide reliability employed in standard silicon technology is the enrichment of the oxide with nitrogen.

In the present work, a systematic study is performed on the thermal oxidation of s-Si at various oxidation conditions as well as nitrogen-enriched thermal oxides fabricated by (a) oxynitridation in N_2O and (b) oxidation of N_2 implanted s-Si. For this scope, electrical characterization, structural characterization and RAMAN spectroscopy as well as computer simulation has been implemented. A wide range of process temperatures has been studied, even at extreme thermal budget processing conditions, in order to explore its applicability limitations in standard CMOS technology. During thermal oxidation of s-Si, it was found that the proximity of the s-Si/SiGe heterointerface to the surface, as the s-Si thickness decreases after oxidation, play an important role on the electrical properties of MOS system (Fig. I.3.2, I.3.3). Similar phenomena appear during N_2O oxidation or oxidation of N_2 implanted samples, however at thicker s-Si thickness, indicating the existence of various physical mechanisms. In all the cases, the oxides show very good electrical properties in term of interface states, breakdown fields, oxide traps and leakage currents. TEM analysis (fig. I.3.4) revealed the absence of defects at the s-Si layer or the graded Si_xGe_{1-x} substrate, even for nitrogen implanted samples, while RAMAN analysis showed that the strain is retained (fig. I.3.5).

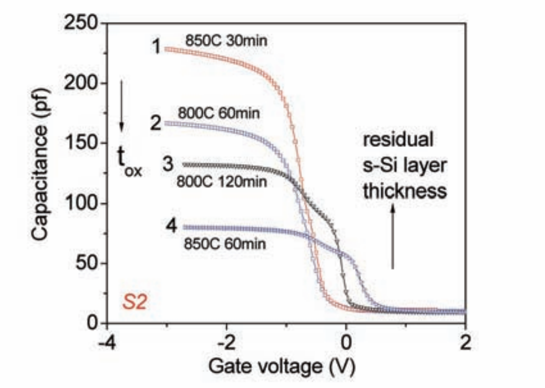


Fig. I.3.2: *CV curves at 1 MHz for various oxidation conditions, demonstrating the appearance of a characteristic hump as the s-Si layer decreases, due to hole confinement phenomena.*

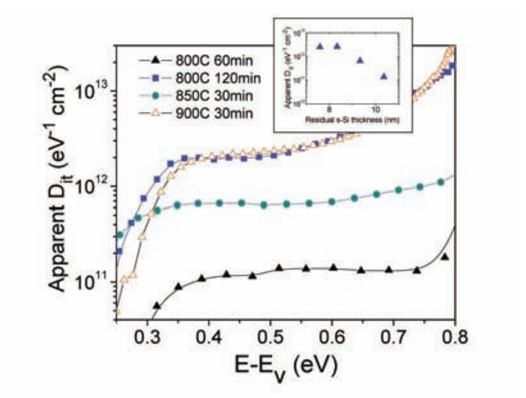


Fig. I.3.3: *Apparent Density of Interface Traps.for conventional s-Si oxidation at various temperatures. Apparent density of traps increases with decreasing s-Si residual layer (inset)*

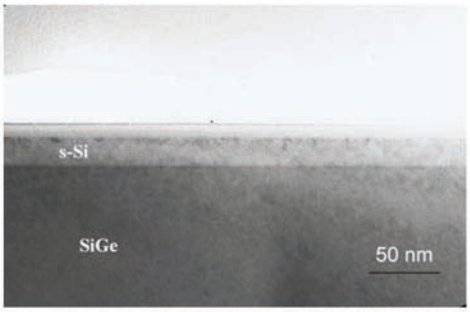


Fig. I.3.4: *TEM image of strained silicon overlayer after N_2 implantation and oxidation. We observe the full absence of extended defects.*

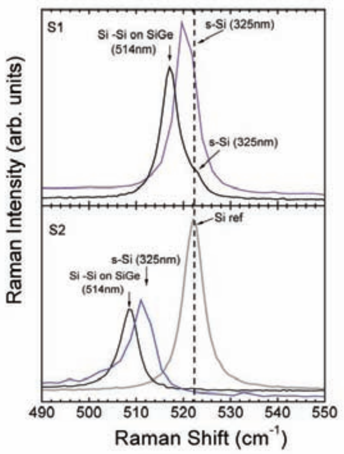


Fig. I.3.5: *Raman spectra collected for s-Si/$Si_{1-x}Ge_x$ specimens using VIS and UV excitations. A spectrum from unstrained Si wafer is also shown, as reference.*

C. Dopant diffusion in Germanium

c_1 Implantation and diffusion of dopants in germanium

A. Chroneos, N. Ioannou, D. Skarlatos and C. Tsamis

Germanium has been an important Group IV semiconductor since its initial use as the first transistor material. Although the mobility of carriers in germanium is higher than that of silicon, its study was soon abandoned due to the lack of a high quality, stable oxide that made it unsuitable for CMOS applications. However, during the last years, it has been demonstrated, that high-quality high–k materials can be deposited by various techniques on germanium substrates arising as promising gate dielectrics for Ge-CMOS applications. As a result, germanium is re-gaining in significance over silicon as a material for future nanoelectronics devices, due to its improved electrical characteristics. For that reason a lot of research efforts have focused the last years in the understanding of the fundamental properties of germanium as well as of phenomena related to the technological processes needed for device fabrication. Unavoidably, dopant diffusion and defect kinetics are expected to play a dominant role in this new technology similar to the silicon technology. It is the aim of this work to study dopant diffusion in germanium and to develop models that can predict the phenomena that take place during these processes.

Germanium wafers were implanted with Phosphorus and Gallium at various doses ($5x10^{13}$ cm^{-2} and 10^{15} cm^{-2}) and a range of energies (30 keV to150 keV). Part of the wafers was covered with a 40 nm silicon dioxide (SiO_2) and an 80 nm silicon nitride (Si_3N_4) capping layer while the rest remained uncovered. The samples were furnace annealed at various temperatures (500ºC-600ºC) and a range of annealing times (30min to 5hrs). The experimental concentration profiles were obtained by Secondary Ion Mass Spectroscopy (SIMS). In the case of uncovered samples, substrate evaporation and significant phosphorous dose loss was observed, depending on the implantation and annealing conditions (Fig. I.3.6). At low implant dose there is insignificant diffusion of phosphorous and gallium in Ge, whereas at the higher implant dose, phosphorous exhibits a "box profile" consistent with previous experimental studies (Fig. I.3.7). Analysis of the experimental results gives important information for the diffusion mechanisms of phosphorus and gallium in crystalline germanium substrates.

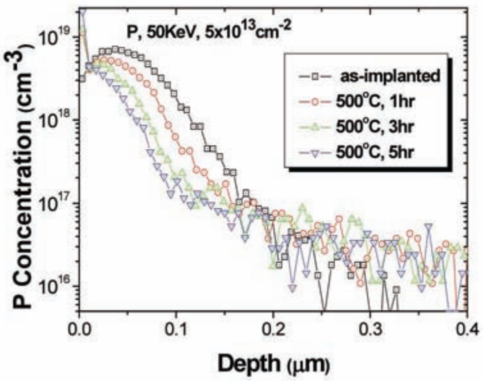


Fig. I.3.6: *Phosphorous concentration for uncapped samples, implanted with a dose of $5x10^{13}$ cm^{-2} and energy of 50 keV after annealing at 500 ºC for various times.*

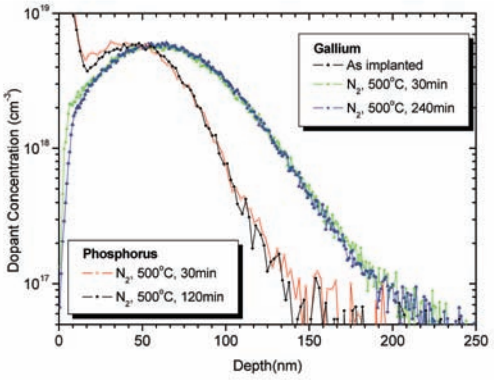


Fig. I.3.7: *Phosphorous and Gallium diffusion after low dose implantation. No significant diffusion is observed for both dopants.*

c_2 *Atomic scale simulations of the Donor-Vacancy complexes in germanium*

A. Chroneos, R. W. Grimes* and C. Tsamis

Atomic scale calculations have been used to predict the structures and relative energies of defect clusters formed between n-type dopants and lattice vacancies in germanium (Ge). These include phosphorous-vacancy (P-V), arsenic-vacancy (As-V) and antimony-vacancy (Sb-V) pairs as well as larger clusters. The calculations used a plane-wave basis set in conjunction with pseudo-potentials within the generalized gradient approximation (GGA) of density functional theory (DFT). Equivalent defects in silicon (Si) are also predicted, and these demonstrate the excellent correlation of the present simulations to previous experimental and theoretical studies. The calculations highlight similarities but important differences in the formation and binding energies of clusters in Ge compared to Si. Interestingly the binding energies of the donor-vacancy pairs do not scale with dopant size.

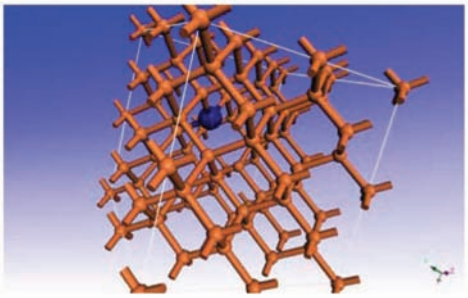
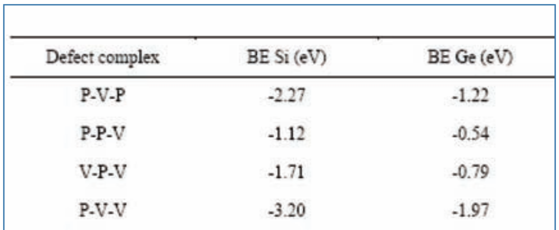


Fig. I.3.8: *A supercell of 62 germanium atoms and a phosphorous-vacancy complex.*



Defect complex	BE Si (eV)	BE Ge (eV)
P-V-P	-2.27	-1.22
P-P-V	-1.12	-0.54
V-P-V	-1.71	-0.79
P-V-V	-3.20	-1.97

Table I: *Total binding energies of the 2P-V and P-2V complexes in Si and Ge*

* *This work is performed in collaboration with the Department of Materials, Imperial College London, UK*

PROJECT OUTPUT in 2006

Publications in International Journals and Reviews

1. "Implantation and diffusion of phosphorous in germanium", A. Chroneos, D. Skarlatos, C. Tsamis, A. Christofi, D.S. McPhail and R. Hung, Mater. Sci. Semicon. Proc., 9, 640-643 (2006)
2. "Atomic scale simulations of donor-vacancy pairs in germanium", A. Chroneos, R. W. Grimes and C. Tsamis, Journal of Materials Science: Materials in Electronics, DOI : 10.1007/s10854-006-9073-8
3. "Atomic Scale Simulations of the As-vacancy Complexes in Germanium", A. Chroneos, R. W. Grimes and C. Tsamis, Materials Science in Semiconductor Processing 9, p. 536–540 (2006)
4. "Oxidation of very low energy nitrogen–implanted strained-silicon", N. Kelaidis, D. Skarlatos, V. Ioannou-Sougleridis, C. Tsamis, Ph. Komninou, B. Kellerman and M. Seacrist, Materials Science and Engineering: B, Volume 135, Issue 3, Pages 199-202, December 2006
5. "Non conservative Ostwald ripening of a dislocation loop layer under inert common and nitrogen – rich SiO_2/si interfaces", D. Skarlatos, P. Tsouroutas, V. Em. Vamvakas and C. Tsamis, J. Appl. Phys. 99 (10): art. no. 103507, May 15 (2006)

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1. "Implantation and diffusion of phosphorous in germanium", A. Chroneos, D. Skarlatos, C. Tsamis, A. Christofi, D.S. McPhail and R. Hung, E - MRS 2006, 29 May-2 June, Nice, France (Oral)
2. "Atomic scale simulations of donor-vacancy pairs in germanium", A. Chroneos, R. W. Grimes and C. Tsamis, Second CADRES Conference, 8-11 September 2006, Crete, Greece (Oral)
3. "Oxidation of very low energy nitrogen–implanted strained-silicon", N. Kelaidis, D. Skarlatos, V. Ioannou-Sougleridis, C. Tsamis, Ph. Komninou, B. Kellerman and M. Seacrist, E - MRS 2006, 29 May-2 June, Nice, France (Poster)
4. "Oxidation of strained–silicon in N_2O ambient", N. Ioannou, D. Tsoromokos, N. Kelaidis, M. Theodoropoulou, S. N. Georga, C. A. Krontiras, D. Skarlatos, C. Tsamis, B. Kellerman and M. Seacrist, E - MRS 2006, 29 May-2 June, Nice, France (Poster)
5. "Atomic Scale Simulations of the As-vacancy Complexes in Germanium", R. W. Grimes A. Chroneos

and C. Tsamis, E - MRS 2006, 29 May-2 June, Nice, France (Poster)

6. "Implantation and diffusion of phosphorous in germanium", A. Chroneos, D. Skarlatos, C. Tsamis, A. Christofi and D.S. McPhail, XXII Panhellenic Conference of Solid State Physics, 24-27 September 2006, Patra (Poster)
7. "Oxidation of strained–silicon in N_2O", N. Ioannou, D. Tsoromokos, N. Kelaidis, M. Theodoropoulou, S. N. Georga, C. A. Krontiras, D. Skarlatos, C. Tsamis, B. Kellerman and M. Seacrist, XXII Panhellenic Conference of Solid State Physics, 24-27 September 2006, Patra (Poster)
8. "Ultra-thin oxide formation on Strained Silicon substrates implanted with very low energy nitrogen", N. Kelaidis, D. Skarlatos, V. Ioannou-Sougleridis, C. Tsamis, Ph. Komninou, B. Kellerman and M. Seacrist, XXII Panhellenic Conference of Solid State Physics, 24-27 September 2006, Patra (Oral)

PROJECT I.4: THIN FILMS by CHEMICAL VAPOR DEPOSITION (CVD)

Project leader: D. Davazoglou

PhD students: G. Papadimitropoulos

Collaborating scientists: Dr. M. Vasilopoulou, Dr. K. Giannakopoulos, N. Vourdas

Funding:

- CONECTOR, "Copper nano-electrodes and novel transistors based on tungsten oxides nano-rods", (GSRT project) 2005-2008
- FOCUS, 2006-2007 (Contract with Industry)

RESEARCH RESULTS

A. Metal-Organic Chemical Vapor Deposition (MOCVD) of Cu films

a_1 Cu thermal deposition over patterned surfaces

G. Papadimitropoulos, D. Renesis

Cu films were deposited by metal-organic chemical vapor deposition (MOCVD) in a newly installed MOCVD reactor with direct liquid injection (DLI) of CupraSelect® (hfacCu^{I}VTMS) vapors. Cu films were deposited on patterned low temperature SiO_2 (LTO) lines 0,5 µm wide and 0,5 µm deep (see Fig. I.4.1). The LTO features were first covered with an LPCVD W film by pyrolysis of $W(CO)_6$ vapors.

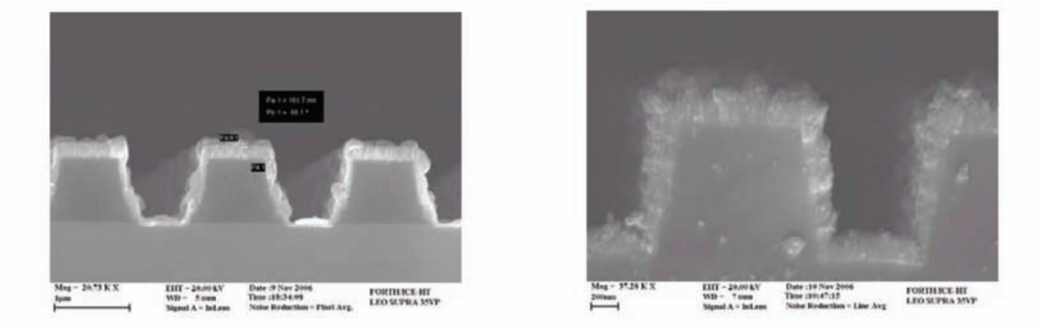


Fig. I.4.1: *LTO features 0,5 µm wide 0,5 µm deep covered with a W/Cu sandwich of films*

a_2 Hot-Wire CVD of Cu - Patterning of Cu films

G. Papadimitropoulos

In Fig. I.4.2a SEM micrograph is shown where Cu is selectively deposited on a patterned insulating WO_3 film at 120°C, (see also below). The deposited film is composed by grains with dimensions of the order of 1 µm. Moreover, it has a resistivity several orders of magnitude higher than that of the bulk metal. When assisted by hot-wire (HWCVD), copper can be easily deposited by CVD on insulating surfaces as shown in Fig. I.4.2 (b,c).

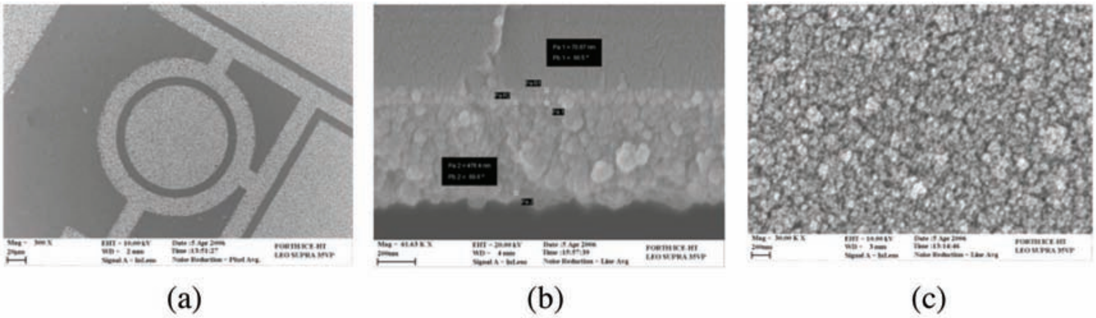


Fig. I.4.2: *(a) Cu deposited selectively on a patterned WO3 film. (b) A sandwich* WO_3*/ hot-wire CVD Cu deposited on a Si substrate. (c) Top view of the Cu film. It is observed that it has a resistivity slightly higher than that of bulk Cu and is fine-grained*

Based on the above a Cu metallization scheme can be proposed within which a WO_3 film is deposited first on a surface patterned with negative-tone photoresist, followed by the deposition of a HWCVD Cu film. The sandwich WO_3/HWCVD Cu is patterned by "lifting-off" the photoresist and the the Cu film thickness is increased further by selective CVD (SCVD) of Cu. The HWCVD Cu layer has low resistivity and smooth surface. A pattern made with this method is shown in Fig. I.4.3.

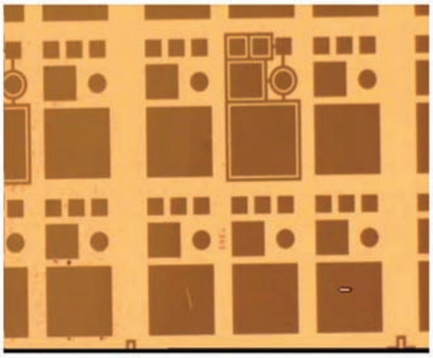


Fig. I.4.3: *Patterns obtained by SCVD of Cu on a lift-off patterned* WO_3*/HWCVD Cu "sandwich".*

B. Nano-structured WO3 thin films of high porosity

b_1 Characterization

G. Papadimitropoulos, N. Vourdas, K. Giannakopoulos

Nano-structured WO_3 films were deposited on quartz substrate by heating a tungsten filament in a vacuum chamber at temperatures of 650, 750 and 800ºC (hot-wire tungsten oxide, hw-TO). Hw-TO films exhibit a very high transmission due to their high porosity. As shown by spectroscopic ellipsometry measurements, porosities above 50% may be obtained (see Fig. I.4.4). TEM measurements have shown that hw-TO films were composed of grains with dimensions of the order of 5 nm. Very small, crystallized regions with dimensions of the order of 3 nm, were also detected.

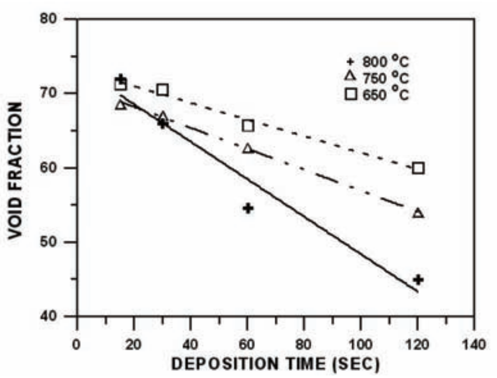


Fig. I.4.4: *Dependence of the porosity of hw-TO films on deposition time for three different filament temperatures.*

b_2 Electrochromic Displays based on WO3 nano-structured films

M. Vasilopoulou, G. Papadimitropoulos and G. Aspiotis

The above described hw-TO films may be deposited on plastic substrates since their deposition takes place at room temperature. In Fig. 8 a polyourethane (PET) sheet covered with a transparent-conductive SnO_2:F layer on which a hw-To layer was deposited is shown. Electrochromic displays were formed by depositing on the PET/SnO_2:F/hw-TO sandwich organic electrolytes and adding a counter electrode of Al. The organic electrolytes were based on poly(methyl methacrylate) (PMMA) and poly(2-hydroxyethyl methacrylate) (PHEMA) into which phospho-11 dodecatungstic acid ($H_3PW_{12}O_{40}$) was added at various concentrations.

The electrochromic configurations formed exhibited high coloration efficiency, near 80 cm^2/Cb as compared to 40 cm^2/Cb for devices based on LPCVD WO3 films. Moreover, they started to color at 0,8 V as compared to 1,5 V and were much faster than devices based on LPCVD WO_3 films.

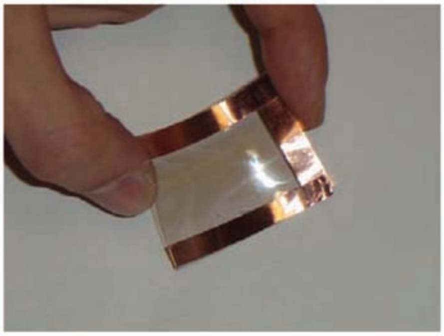


Fig. I.4.5: *A hw-TO film deposited on a PET substrate covered with a SnO_2:F layer.*

C. Colloidal Lithography

L. Zambelis

Monodispersed spheres of submicron to micron sizes can self-assemble into highly ordered and close-packed arrays, so-called colloidal crystals. By using the ordered interstitial arrays within colloidal crystals as masks, one can succeed in sculpturing hexagonal arrays of monodisperse nanoparticles with the shape of a pyramid, ring, or rod on planar substrates, paving a colloidal lithography way. This enables rather facile and cheap fabrication of periodic nanostructures over large areas as compared to conventional lithography. In Fig. I.4.6 (left) an array of hexagonally closely packed polystyrene (PS) spheres with dimensions of 0,9 µm is shown. This array can be used as template for the subsequent vacuum deposition of metal nano-dots as shown in Fig. I.4.6 (right) where periodically arranged Cu nano-dots with dimensions of the order of 200 nm are shown.

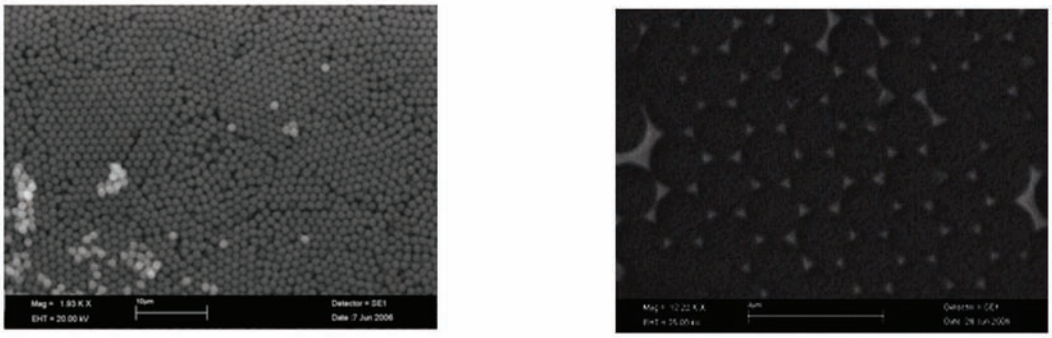


Fig. I.4.6: *(Left) SEM image of hexagonally packed PS spheres with dimension of 0,9 μm. (Right) a periodic arrangement of Cu nano-dots with dimensions of 200 nm produced after vacuum evaporation of the metal through a mask such as that shown left and etching of the PS spheres (the diameter of PS spheres was 1,3 μm).*

D. Selective CVD of Vanadium oxide films

E. Kritikos, L. Zambelis

Vanadium oxide films were deposited by atmospheric pressure chemical vapor deposition (APCVD) on Si substrates covered with Cu films by oxidizing Vanadium (V) tri-i-propoxy oxide ($OV(OC_3H_7)_3$) vapors. Selective deposition on Cu was carried out at atmospheric pressure and at temperatures varying between 135 and 350 °C. The Vanadium oxide films were characterized by X-ray diffraction and electrical resistance measurements at various temperatures.

Electrical resistance measurements made at temperatures varying between 25 and 80 °C have shown that APCVD VOx films exhibit an insulator to metal transition at 68 °C. The exact point of this transition depends on the temperature of deposition, which, as shown by XRD measurements, implies changes in the stoichiometry of films.

Selective APCVD of VO_x combined with colloidal lithography yields ordered features in the nano-scale as shown in Fig. I.4.7.

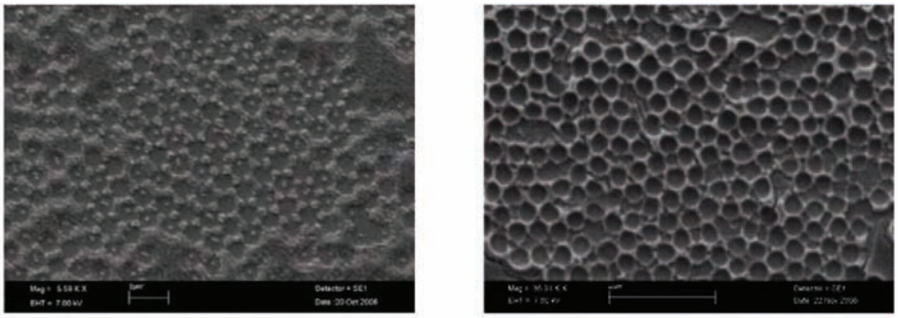


Fig. I.4.7: *Nano-scale features obtained by selective APCVD of VOx on Cu patterned with colloidal lithography.*

PROJECT OUTPUT in 2006

Publications in International Journals

1. "Optical and structural properties of copper oxide thin films grown by oxidation of metal layers", G. Papadimitropoulos, N. Vourdas, V. Em. Vamvakas and D. Davazoglou, Thin Solid Films, 515, 2428 (2006)
2. "Polymeric electrolytes for WO_3-based electrochromic displays", M. Vasilopoulou, I. Raptis, P. Argitis, I. Aspiotis and D. Davazoglou Microelectronics Engineering 83 (4-9 SPEC. ISS.), pp. 1414-1417, (2006)

M.Sc. theses

1. E. Kritikos, "Structure and electrical properties of CVD vanadium oxide films", UOA July 2006
2. D. Renesis, "Deposition of W/Cu layers on patterned LTO surfaces. Study of the dependence of step coverage on the deposition conditions", UOA Dec. 2006

Research Programme II

NANOSTRUCTURES & NANOELECTRONIC DEVICES

PROJECT II.1: NANOSTRUCTURES FOR NANOELECTRONICS AND PHOTONICS

Project leader: A. G. Nassiopoulou

Key researchers: A. G. Nassiopoulou, E. Tsoi, S. Gardelis and N. Papanikolaou

Phd students: M. Kokonou, A. Olziersky, A. Salonidou, A. Zoy, V. Gianneta

Funding:

- EU IST NoE SINANO, 1/1/2004-31/12/2006, Contract No: 506844
- EU IST NoE MINA-EAST, 1/5/2004-30/4/2006, Contract No: 510470
- EU IST I_3 ANNA, 1/12/2006 – 1/12/2010, Contract No: 026134

Research orientation:

- Semiconductor (Si, Ge) nanostructures: Growth by LPCVD and sputtering, characterization: electrical, optical, structural
- Si/Ge nanocrystal non-volatile memories
- Ultra-thin porous alumina template technology on silicon. Application in through-pore silicon nanostructuring
- Self-assembly of quantum dots on nanostructured surfaces
- Theory (Ballistic transport in nanostructures, Surface plasmons in thin metallic films, classical molecular dynamics and nanoscale heat transport)

The activity on semiconductor nanostructures started at IMEL at the early nineties and it was conducted within different EU projects, in collaboration with other European groups (Esprit-EOLIS, IST FET SMILE No 28741, IST FORUM FIB No 29573, IST NoE SINANO etc). Worldwide original results were produced, including fabrication of light emitting silicon nanopillars by lithography and anisotropic etching and investigation of their properties, growth of Si nanocrystal superlattices by LPCVD and high temperature oxidation/annealing with interesting optical properties, fabrication and characterization of LEDs based on Si nanopillars, nanodots and others.

The present focus of research is on self-assembly and ordering of Si and Ge quantum dots on nanostructured silicon surfaces and their application in nanocrystal memories and photonics. For Si nanostructuring, a non-lithographic process using porous alumina template technology has been developed. Porous alumina ultra-thin films are grown on silicon by electrochemistry. By appropriately choosing the electrochemical conditions used, pore size and density are monitored. Through-pore silicon nanostucturing follows the pore size and density. Arrays of SiO_2 nanodots on Si were fabricated and characterized. Dot size varies from few nm up to few hundreds of nm.

Another technology under development is the growth of ultra thin porous silicon films by electrochemical dissolution of silicon in the transition regime between porosification and electropolishing. Under appropriate conditions, the obtained films are amorphous with embedded Si nanocrystals of various sizes. Under other conditions, the films are nanocrystalline.

Characterization of nanostructures includes investigation of their optical, electrical and structural properties.

The theoretical group focuses on the investigation of ballistic transport in nanostructures, surface plasmons in thin metallic films, classical molecular dynamics and nanoscale heat transport.

A brief overview of the main results obtained in 2006 is given below.

RESEARCH RESULTS

A. LPCVD growth of double-layers of silicon nanocrystals within the gate dielectric of a MOS structure for improved non-volatility in nanocrystal memories

A Salonidou and A. G. Nassiopoulou
In collaboration with K. Giannakopoulos and A. Travlos from the Institute of Materials Science for TEM work

Layers of silicon nanocrystals embedded in SiO_2 are fabricated in this work by low-pressure chemical vapor deposition (LPCVD) of amorphous Si, followed by high temperature thermal oxidation and annealing. The thickness of the amorphous layer as well as the oxidation time are adjusted so as to get the desired thickness of the nanocrystal layer and the top oxide. The main advantage of this process are the tunability of nanocrystal size and the good quality of barrier silicon oxide.

By using the above process, single and double layers of silicon nanocrystals were fabricated within the gate dielectric of a MOS memory structure.

By using doubly-stacked dots layers (fig. II 1.1 a,b), with a smaller dot with diameter below ≈3nm underneath a larger one, of size ~5nm, it is possible to create a barrier to carriers from the dot to the silicon substrate, as indicated schematically in fig. 7a. This structure is expected to improve data retention in the low voltage regime due to the band offset between the two dots, induced by more pronounced quantum-confinement bandgap opening in the smaller dot compared to the larger one, as shown schematically in fig II.1.1c.

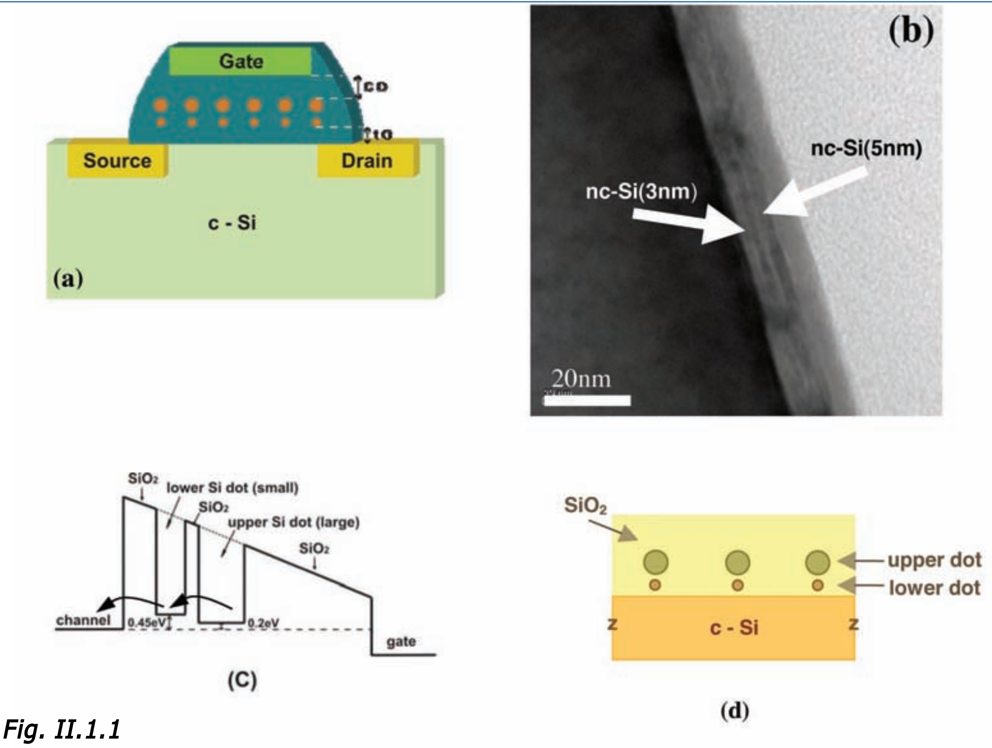
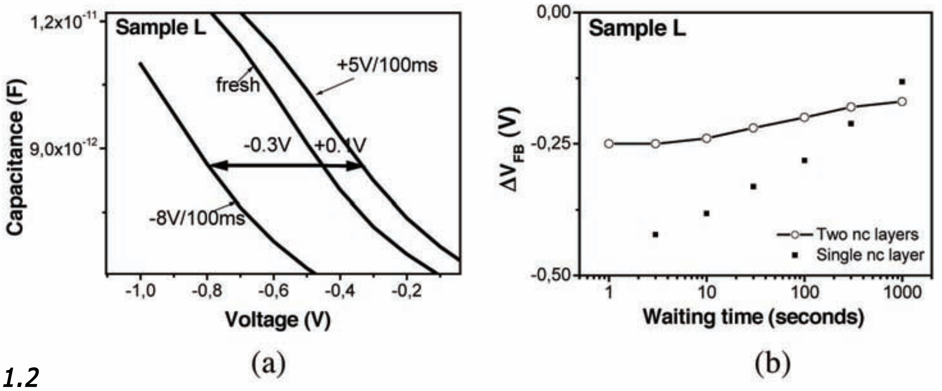


Fig. II.1.1

A sample structure as in fig. II.1.1b was used to fabricate nanocrystal MOS capacitors that have been characterized for their charging properties by electrical measurements. Double-dot-layer structures showed much slower charge loss at zero bias compared with similar structures with a single nanocrystal layer. This is illustrated in fig. II.1.2. In (a) we see the shift in C-V curves after application of a positive (+5V/100ms) or negative (-8V/100ms) pulse on the gate of a device with the following gate dielectric structure on p-type silicon: tunnel oxide 3.5nm/NC_1-d=3nm/inter-dielectric:1.5nm/NC_2-d=5nm/control oxide:8nm. The retention characteristics (ΔV_{FB} versus time) after writing at -8V/100ms are shown in fig. II.1.2B (open circles). In the same graph we show in full squares the retention characteristic of a similar single-dot-layer device with nanocrystal size d=3nm. In this second case, under the same charging conditions the maximum shift in VFB is larger, but charge loss is much faster.



(a) (b)

Fig. II.1.2

B. Growth of ultra-thin anodic Si films for optoelectronic and nanoelectronic applications

S. Gardelis and A.G. Nassiopoulou

We developed a method for fabricating ultra-thin (18-80 nm) light emitting films with embedded silicon nanocrystals by anodization of bulk crystalline Si in the transition regime between porocification and electropolishing using short mono-pulses of anodization current. The size of the nanocrystals decreased with increasing current density and it was in the range of 3-7 nm with current densities in the range of 130-390 mA/cm^2. At the highest current densities used the film/substrate interface was very sharp (Figure a), while at lower current densities the interface contained nanostructured silicon spikes protruding from the substrate into the nanostructured film. All the investigated films exhibited broad photoluminescence at room temperature at around 630 nm (Figure b). The photoluminescence intensity increased considerably with increasing anodic current density in the transition regime (up to 100 times in the films we studied), whereas thickness of the corresponding films increased by only three times. We attributted the effect of intense light emission to quantum confinement in the smaller Si nanocrystals embedded in these films (smaller than 2nm). The growth of such films is investigated due to their potential use in optolectronic and nanoelectronic applications.

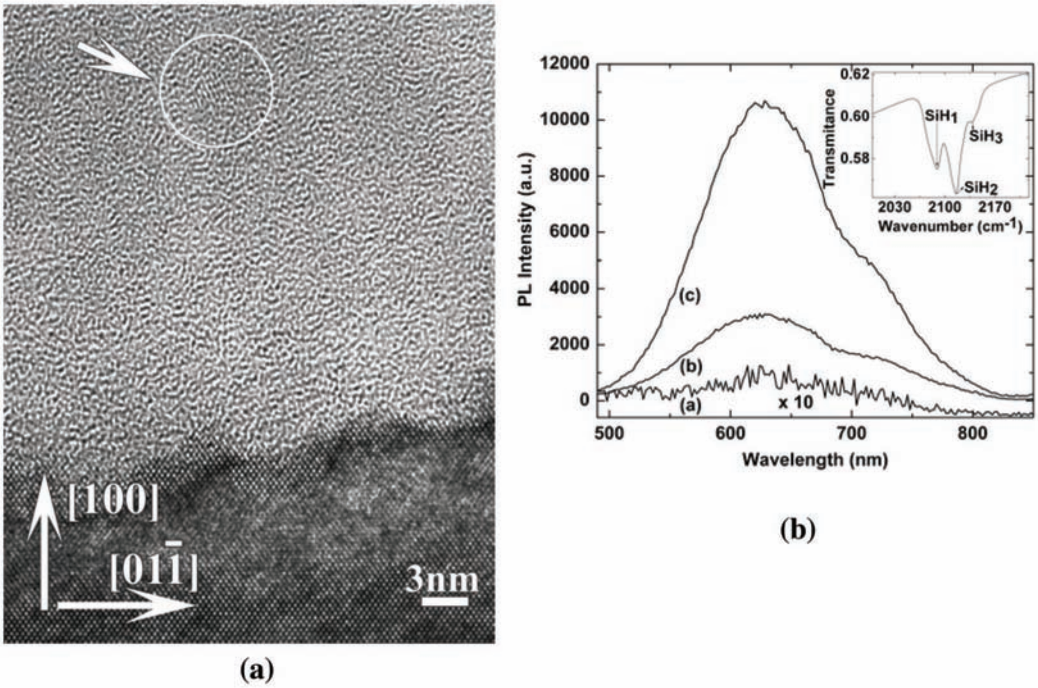


Fig. II.1.3: ***(a)*** *HREM image obtained from the film grown at the highest current density used, showing a smooth interface and Si nanocrystals embedded in an amorphous matrix.* ***(b)*** *Photoluminescence obtained from the films at room temperature . The inset depicts FTIR spectrum obtained from the films, showing the presence of Si-H_x vibrational modes at the film surfaces.*

C. Ultrafast transient photoinduced absorption in silicon nanocrystals: Coupling of oxygen-related states to quantized sublevels

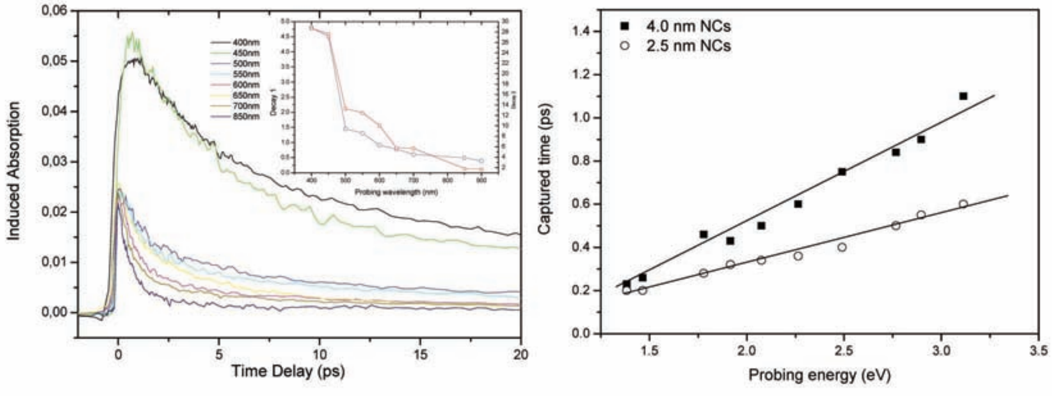
Emmanouil Lioudakis[1], A. Othonos[1], A. G. Nassiopoulou

[1] Collaborators from the University of Cyprus

We have studied transient photoinduced absorption (TPA) in single monolayers of oxidized Si-NCs embedded in amorphous SiO_2 matrix with two different NC sizes (2.5 and 4nm). The experimental TPA measurements along with optical absorption measurements reveal that the light-absorption process takes place inside the Si-NC band structure, suggesting that the photoexcited carriers are in oxygen-related states. From our experimental results, we observe two different relaxation mechanisms/channels for the free carriers at the first few picoseconds before radiative recombination (PL). Probing at different energy states, we suggest that for both NC sizes the fast relaxation mechanism corresponds to the internal relaxation of oxygen-related states at the interface of Si-NCs with SiO_2. The slower relaxation process may be correlated with quantized sublevels which are formed due to the embedded NCs in the SiO2 matrix.

As an example, in fig. II.1.4a, we present the experimental data of TPA of the larger Si-NCs (4 nm) following optical excitation around the oxygen-related states (400 nm) at different probing wavelengths ranging from 400 to 900 nm. These data were obtained from the combination of the temporal reflectivity and transmittance changes of the sample. After the excitation the photogenerated carriers populate the electron/hole oxygen-related states. As the carriers relax a coupling to higher energy states (induced absorption) is achieved due to the probing pulse.

Due to the strong correlation of the oxygen-related states of these materials, effects at lower energy states such as state filling do not appear in our measurements. The initial fast rise of experimental results corresponds to the effective time [$\tau_0(\lambda)$] until an efficient coupling has been achieved. This time is a basic characteristic for each material and is directly related to the initial carrier density as well as the opened optical channels at the particular energy difference (probing energy resonance). In fig. II.1.4b, we present this effective time as a function of the probing energy. As seen from these results, the time increases linearly with the probing energy. This means that with increasing probing energy, the coupling has been achieved at longer times. The latter is attributed to the reduced wave function overlapping between the coupled energy states.



(a) (b)

Fig. II.1.4: (a) *(Color) Ultrafast TPA measurements from 4 nm Si-NCs at different probing wavelengths. The inset shows both fast and slow relaxation times as a function of probing wavelength (400-900 nm).* ***(b)*** *Effective time as a function of the probing energy for both Si-NC sizes. The lines are the linear fits in the experimental data.*

D. Fabrication of SiO2 quantum dots on Si substrates through thin films of porous alumina. Their use in Si nanopatterning

V. Gianneta, M. Kokonou and A. G. Nassiopoulou

SiO_2 nanostructures on silicon substrates are attracting interest because they exhibit very useful properties for various applications in nanoelectromechanical systems (NEMS) and nanoelectronic devices. Nanostructuring of silicon through the pores of anodic alumina is a promising technique due to the low cost and the simplicity of the whole experimental procedure.

In this work, regular arrays of SiO_2 quantum dots were fabricated on silicon through alumina pores. Porous alumina thin film on Si constitute a very interesting material fabricated by anodization of Al films under certain electrochemical conditions that lead to self-organization of the film and formation of regular vertical pores arranged in an hexagonal close-packed structure. The SiO_2 dots start to form during anodization after total aluminum consumption, when the electrolyte reaches the Si substrate. The size and density of the quantum dots depend strongly on the electrochemical conditions applied and the structural characteristics of the porous alumina layer.

The SiO_2 dots are homogenous in diameter and height and their arrangement follows the initial hexagonal structure of the porous alumina layer.

We fabricated arrays of dots with size that varied from 2-10 nm in height and 10-30 nm in diameter.

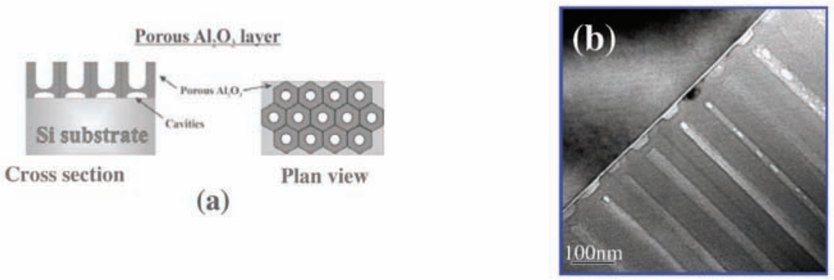


Fig. II.1.5: ***(a)*** *Schematic representation of a cross section and a plan view of porous alumina thin film on Si.* ***(b)*** *TEM image of porous alumina thin film (cross section) on Si*

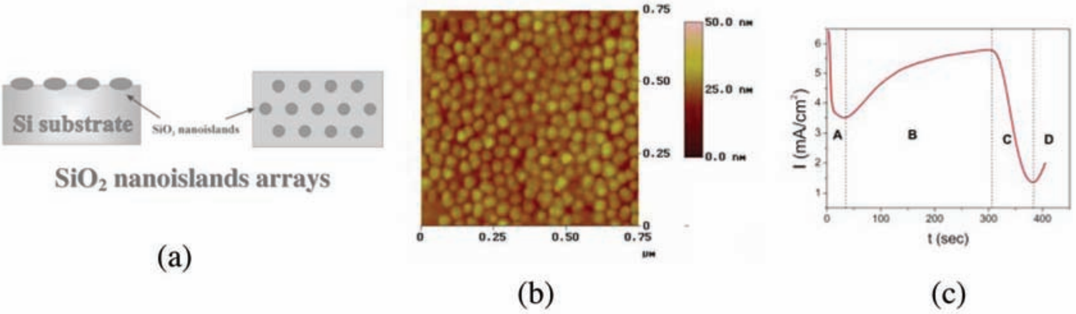


Fig. II.1.6: ***(a)*** *Schematic representation of SiO_2 dots on Si (cross section and plan view).* ***(b)*** *AFM image of an array of such dots on Si.* ***(c)*** *Example of anodization curve.*

By removing the SiO_2 dots, we obtain a nanopatterned Si surface (bare or oxidized), which is appropriate for self-assembly of nanodispersed Si or Ge quantum dots.

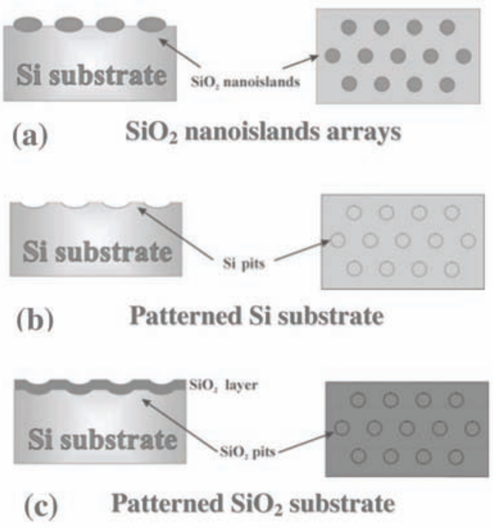


Fig. II.1.7: *Successive steps for Si nanopatterning.* ***(a)*** *Arrays of SiO_2 dots fabricated through porous anodic alumina.* ***(b)*** *Nanopatterned bare Si surface after removal of the dots.* ***(c)*** *Nanopatterned oxidized Si surface (oxidation of the nanopatterned surface shown in (b))*

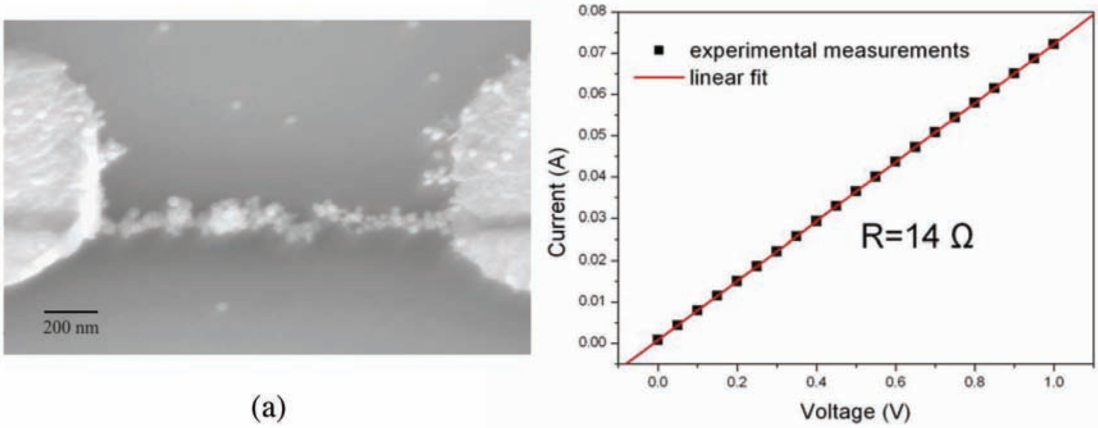
E. Self assembly of gold nanoparticles by dielectrophoresis

A. Zoy and A.G. Nassiopoulou

In this work we developed the dielectrophoresis technique for controllable and rapid assembly of Au nanostructures between electrodes. This technique is based on the force exerted on the induced dipole moment of a dielectric or conductive particle by a non-uniform electric field. Alternative (AC) electric fields are often preferred in order to suppress electrochemical reactions, as for example electrolysis at the electrodes surface and to overcome the limitation of strong surface particle charge. DEP is suitable for microfluidic applications and nanoassembly.

At IMEL, dielectrophoresis has been used for the controllable assembly of gold nanoparticles between electrodes and the formation of conductive nanowires with micrometer length. Different aqueous colloidal gold nanoparticles with average diameter of 20, 30, 40 and 45 nm were assembled between gold or platinum electrodes with 1 μm distance between them placed on a 150 nm thick SiO_2 layer. The effect of the frequency and strength of the applied field on the particle accumulation process was investigated. Two typical results at low and higher frequency including SEM images and corresponding current-voltage characteristics are shown in fig.II.1.8.

At low frequencies, the Au nanoparticles are aggregating and the corresponding I-V characteristic is polynomial, which is indicative of space charge limited conductivity of the structure. At higher frequencies, the Au nanoparticles are deposited in a discrete way as shown in fig. II.1.8(a). In this case, samples exhibit linear conductivity with the applied voltage. An example is given in fig. II.1.8b. In this case the transport mechanism is hopping conductivity.



(a)

(b)

Fig. II.1.8: *SEM image of a single Au nanoparticle chain formed by dielectrophoresis between micron-distant electrodes, with V-groove lines between the electrodes. The applied ac electric field had an amplitude of 3 V at 2 kHz. In (b) we see an example of current-voltage characteristic of the nanoparticle chain and the corresponding linear fit from which a chain resistance of 14 Ω is deduced.*

F. Ballistic transport in nanostructures

N. Papanikolaou

As modern electronic devices are getting close to 10 nm in dimensions there is a growing interest in alternative technologies which will replace Si. Understanding electronic transport in the atomic scale is an important milestone towards this goal. We have investigated theoretically the ballistic electronic conductance through single atoms attached to Cu and Pd crystalline electrodes. We use state of the art ab *initio* electronic structure methods based on density functional theory. We have systematically studied different contacts and different leads. One important conclusion is that the conductance of the system is mainly determined by the electronic properties of the atom bridging the leads. The contact geometry is crucial only when transition metal atoms are present in the contact. Our calculations offer a transparent physical picture in accordance with recent experimental reports.

f_1 *Surface plasmons in thin metallic films*

Surface plasmon excitation is responsible for many interesting phenomena in optics like extraordinary transmission through metal films with sub-wavelength hole arrays, surface enhanced Raman scattering and negative refraction. There are also interesting potential applications in building optical filters and sensors as well as subwavelength optical waveguides. We study surface plasmons in thin films decorated with metallic sphere arrays. We focus on the interaction between flat surface plasmon- polaritons and particle plasmons. Maxwell's equations are solved exactly using a multiple scattering formalism which combines high accuracy with efficiency. Light transmission through such structures can be enhanced by an order of magnitude.

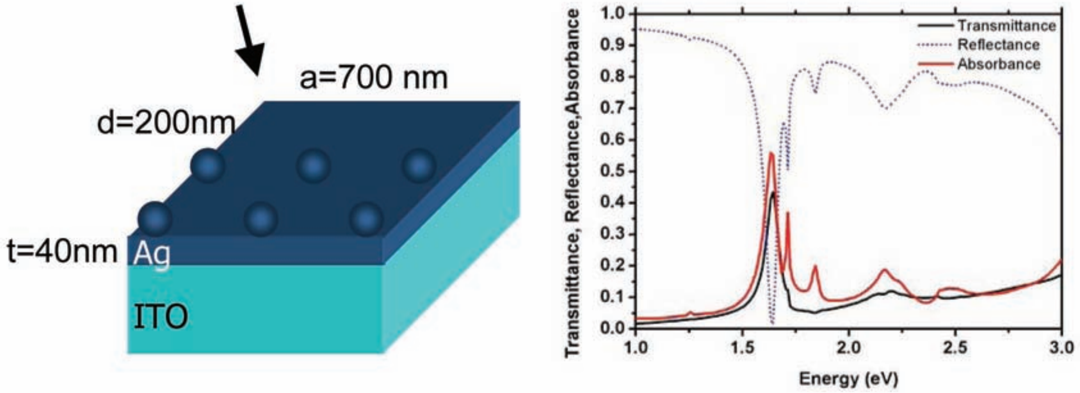


Fig. II.1.9: *Left panel: Schematics of a square array of metallic spheres (diameter 200nm, lattice constant 700 nm) on a 40 nm thin Ag metallic film on top of indium tin oxide (ITO) substrate. Right panel: Transmission, Reflection and absorption through the system depicted on the left. For photon energy close to 1.6 eV, transmittance is almost 45%.*

In the system shown in the figure the presence of the sphere array increases the transparency of the film by a factor 10 compared with the system without the spheres. Similar results have been reported before in systems with periodic arrays of particles on both sides of the film, and where confirmed experimentally. The presence of a high refractive index dielectric like ITO in this case allows the leakage of light without the need of periodic structures on both sides of the film. Our aim is to use these results in the design of new, highly sensitive, optical sensors.

f_2 *Classical molecular dynamics and nanoscale heat transport*

We have developed a new classical molecular dynamics computer code appropriate for semiconductor materials. Our implementation includes an energy minimizer and the molecular dynamics. We have implemented several classical potential parameterisations like, Stilliger-Weber, Tersoff, EDIP, for Si, Ge, and C, embedded atom method potentials to use in metallic systems as well as metal semiconductor interfaces. A few silicon dioxide potentials are also available.

Provided the potential is available, the method can be used for a variety of problems like calculation of local pressure and tension in nanostructures, diffusion, oxidation, growth etc. We have first applied the method in the calculation of the thermal conductivity of SiC nanowires. We use a non equilibrium molecular dynamics method by creating a heat flux along the nanowire, and calculating the resulting temperature gradient. Our results show that thermal conductivity is greatly reduced compared to the bulk SiC which is mainly due to scattering at the nanowire surface.

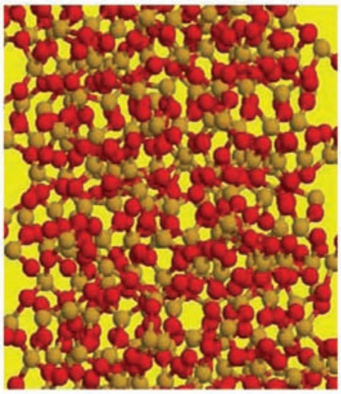


Fig. II.1.10: *Amorphous SiO_2 snapshop from MD simulation*

PROJECT OUTPUT in 2006

Publications in Refereed Journals

1. "Photoluminescence lifetimes of Si quantum dots", Xanthi Zianni and A. G. Nassiopoulou, J. Appl. Phys. 100, 074312 (2006)
2. "Growth and characterization of high density stoichiometric SiO2 dot arrays on Si through anodic porous alumina template", M. Kokonou, A. G. Nassiopoulou, K. P. Giannakopoulou, A. Travlos, T. Stoica and S. Kennou, Nanotechnology 17, 2146 (2006)
3. "Probing carrier dynamics in implanted and annealed polycrystalline silicon thin films using white light", E. Lioudakis, A. Othonos and A. G. Nassiopoulou, Appl. Phys. Lett. 88 (18) 181107 (2006)
4. "Femtosecond carrier dynamics in implanted and highly annealed polycrystalline silicon", E. Lioudakis, A. G. Nassiopoulou, A. Othonos, Semicond. Sci. & Techn. 21 (8), pp. 1041-1046 (2006)
5. "Ellipsometric analysis of ion-implanted polycrystalline silicon films before and after annealing", E. Lioudakis, A. G. Nassiopoulou and A. Othonos, Thin Solid Films 496 (2), pp. 253-258 (2006)
6. "Ge quantum dot memory structure with laterally ordered highly dense arrays of Ge dots", A. G. Nassiopoulou, A. Olzierski, E. Tsoi, I. Berbezier and A. Karmous, J. Nanosci. Nanotechnol., vol. 7, 316-321, 2007 (on line 2006)

7. "Two-silicon-nanocrystal layer memory structure with improved retention characteristics", A. G. Nassiopoulou and A. Salonidou, J. Nanosci. Nanotechnol., vol. 7, 368-373, 2007 (on line 2006)
8. "Ab initio approach to the ballistic transport through single atoms", A. Bagrets, N. Papanikolaou, and I. Mertig, Phys. Rev. B 73, 045428 (2006)

Publications in Conference Proceedings

1. "Photoluminescence from silicon nanocrystals formed by anodization of bulk crystalline silicon in the transition regime", S. Gardelis, A.G. Nassiopoulou, Proceedings of the 5th International Conference on Porous Semiconductors-Science and Technology (PSST), Sitges-Barcelona, 12-17 March, 2006

Conference Presentations

1. "Fabrication of ordered SiO_2 dots on Si substrate through a porous alumina thin film", V. V. Gianneta, M. Kokonou and A. G. Nassiopoulou, XVIII Greek Conference on Solid State Physics and Materials Science, Patra, September 2006
2. "High density of silicon nanocrystals nucleated on oxidized or non-oxidized stepped silicon substrates patterned by electrochemistry", M. Kokonou, A. G. Nassiopoulou and K. P. Giannakopoulou, European Materials Research Society Spring Meeting (E-MRS), Nice, France, May 29 – June 2, 2006
3. "Doubly stacked silicon nanocrystal memory structures with improved charge retention time", A. G. Nassiopoulou and A. Salonidou, European Materials Research Society Spring Meeting (E-MRS), Nice, France, May 29 – June 2, 2006
4. "Photoluminescence properties and passivation of thin porous silicon films grown in the transition regime", S. Gardelis and A. G. Nassiopoulou, European Materials Research Society Spring Meeting (E-MRS), Nice, France, May 29 – June 2, 2006
5. "Quantum confinement and interface structure of large Si nanocrystals embedded in a-SiO_2", E. Lioudakis, G. C. Hadjisavvas, P. C. Kelires, A. G. Nassiopoulou and A. Othonos, European Materials Research Society Spring Meeting (E-MRS), Nice, France, May 29 – June 2, 2006

Invited Talks

1. "Semiconductor quantum dots for nanoelectronic devices and on-chip integration", A. G. Nassiopoulou (Invited Talk), third Workshop on functional materials, FMA 2006, September 17-23 2006, Athens, Greece
2. "Micro-Nanoelectronics-Nanotechnology. The world of the infinitely small", A. G. Nassiopoulou (Invited Talk), 4th International Student Conference of the Balkan Physical Union, ISCBPU-4, Bodrum, 29/8-1/8/2006
3. "Lateral ordering of semiconductor nanocrystals within SiO2 for non-volatile memories and other nanoelectronic devices", A.G. Nassiopoulou (Invited Talk), NANOMAT-2006, Antalya, 21-23.6.2006
4. "Silicon nanocrystal non-volatile memory devices", A. G. Nassiopoulou (Invited Talk), SINANO Workshop, Montreux, 22/9/2006
5. "Lateral ordering of semiconductor nanocrystals within SiO2 for nanoelectronic devices", A. G. Nassiopoulou (Invited Talk), 3rd Workshop N&N, Thesssaloniki, 10-12 July 2006
6. "Light emission from silicon: Reality or dream?", A. G. Nassiopoulou (Invited Talk), 1st International Workshop on Transparent Conductive Oxides (IS-TCO 2006), Crete, 23-25 October, 2006

7. "Lateral ordering of semiconductor nanocrystals for memory applications", A. G. Nassiopoulou (Invited Talk), Workshop on Silicon Nanodevices Beyond CMOS: Emerging Nanodevices, RWTH Aachen, Germany, 7 – 8 November 2006
8. "Microelectronics-Nanotechnology: Present status and future trends", A. G. Nassiopoulou (Invited Lecture), University of Thessaloniki, 18/10/2006
9. "Quantum wires and dots, applications in Nanoelectronics and sensors", A. G. Nassiopoulou (Invited Lecture), University of Thessaloniki, 18/10/2006

Organisation of Conference

1. E-MRS IUMRS ICEM 2006 Spring Meeting – Organization of Symposium C: Silicon nanocrystals for nanoelectronics and sensors, Nice 29/5 – 2/6/2006, Chairpersons: A. G. Nassiopoulou, Ph. Fauchet, L. Lechuga, Edition of Proceedings to appear in Physica E

PhD theses

1. "Nanocrystalline silicon for application in non-volatile memories", Doctoral thesis of A. Salonidou, Univerity of Athens 17/4/2006
2. "Arrays of semiconductor nanocrystals ordered in 2-D layers within SiO2 for application in memory devices", PhD thesis of A. Olzierski, Univerity of Athens 6/10/2006

PROJECT II.2: NANOCRYSTAL MEMORIES

Project leader: Dr P.Normand

Key researchers: Dr P. Normand, Dr V. Ioannou-Sougleridis

Collaborating researchers: Dr. P. Argitis, Dr. M. Chatzichristidi, Dr. J. Raptis

Post-doctoral: Dr V. Vamvakas

PhD candidate: P. Dimitrakis

Objectives:

- To develop novel high-throughput synthesis routes and techniques for creating nanostructured materials in dielectrics, such as Si nanocrystals in SiO_2 films by low-energy ion-beam-synthesis.
- To investigate the structural and electrical properties of the generated nanostructured materials and demonstrate material characteristics enabling the development of low-voltage high-density memory devices.
- To realize and evaluate nanostructure-based-memory devices and assess the manufacturability of the developed nanofabrication routes in an industrial environment.

Funding

- NEON, Nanocrystals for Electronic Applications, EU GROWTH GRD1, No 25619
- Bilateral French-Greek Project, Si-Nanocrystal Synthesis by Plasma-Immersion Ion-Implantation for Non-Volatile Memory Applications, ΕΠΑΝ. Μ.4.3.6.1Ε.

Activities:

By associating the finite-size effects of nanocrystals and the benefits of a stored charge distribution, the nanocrystal memories (NCMs) have the potential to fulfill the stringent requirements of non-volatile memory cell downscaling. Our activities in this area started in 1996 through the development of the low-energy ion-beam-synthesis (LE-IBS) technique for producing nanocrystals in thin gate dielectrics. This activity was supported by the EU project, FASEM (1997-2000). LE-IBS development with target the realization of manufactory non-volatile NCMs has been conducted within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last four years for developing novel NCMs alternatives including, (a) Memory devices by Si^+ irradiation through poly-Si/SiO_2 gate stack in collaboration with FZR and ZMD Dresden, (b) Memory devices using Ge nanocrystals produced by MBE and rapid-thermal processing in collaboration with Aarhus Univ., (c) hybrid silicon-organic and SiGe-organic memories in collaboration with Durham Univ.; this last activity was conducted within the framework of the EU IST-FET project, FRACTURE (2001-2003).

In 2006, our main activities were focused on the following four tasks:

1. Block-copolymer-assisted-nanostructure fabrication for memory applications
2. Ge nanocrystals in high-k dielectrics obtained by low-energy ion-beam-synthesis
3. Channel edge effects in shallow-trench-isolated nanocrystal memories
4. Oxide/nitride/oxide (ONO) dielectric stacks with Si nanocrystals embedded in nitride

During 2006, activities aiming at the development of a Si-NC synthesis route based on plasma-immersion ion-implantation (PIII) in collaboration with CEMES/CNRS and one French SME (Ion Beam Services) were initiated. Our group was also involved in research activities conducted at NTUA (Prof. D. Tsoukalas) regarding NCM radiation hardness.

Specific targets for 2007 include: (a) Fabrication of nanostructures by block-copolymer nanopatterning in collaboration with project I.1, (b) formation of ONO dielectric stacks by LE-IBS for producing SONOS devices at low-thermal budgets, (c) design and fabrication of organic memories in collaboration with project II.1, (d) development of the PIII technique for Si-NC fabrication.

RESEARCH RESULTS

A. Block-copolymer-assisted-nanostructure fabrication for memory applications

P. Normand, K. Parisiadis, A. Avgeropoulos, P. Argitis, M. Chazichristidi, J. Raptis, G. Boulousis

The physical and technical problems associated with lithographically defining nanostructures have opened opportunities for self-assembling physical systems to play a role in preparing nanomaterials. While several self-assembly techniques (e.g. LPCVD, ion-beam-synthesis, aerosol deposition, MBE) have been tested, they fail to meet the requirements of controlled nanostructure-size, -shape, -interspacing and -density. Development of novel nanofabrication routes able to meet these requirements and their application to the production of functional nanostructures is highly desirable. Such a development constitutes the overall aim of the present task that follows a nanofabrication strategy based on block-copolymer (BC) self-assembly for nanopatterning.

BCs self-assemble into a variety of ordered structures via microphase separation. Nanostructure shapes, sizes and inter-spacing are readily tailored through the volume fraction of one of the components, macromolecular architecture, molecular weight of the different blocks and blending of the copolymer with one or more homopolymers. Proper choice of the chemical nature of the constituent blocks in combination with a variety of decomposition methods allows for the selective removal of one of the phases of the precursor material thus leading to long-range ordered nanopatterns. These nano-patterns can then be transferred to underlined substrate materials using advanced etching and deposition/growth techniques, so that nanostructures of practically any semiconductor, dielectric, metal or ferromagnetic material can be formed.

In this direction, our 2006-activities concentrated on two objectives: (1) Generation of in-plane oriented nanoscopic PMMA cylindrical domains in polystyrene materials using two asymmetric diblock copolymer P(S-b-MMA) systems. (2) Removal of the PMMA domains using selective decomposition methods for the purpose of nanoporous PS film formation. Substantial efforts were devoted on substrate preparation and diblock copolymer (DC) process parameters that can affect the size, density, orientation and ordering of the cylindrical domains. Nanoporous PS films have been successfully achieved onto Si, SiO_2 and Si_3N_4 materials.

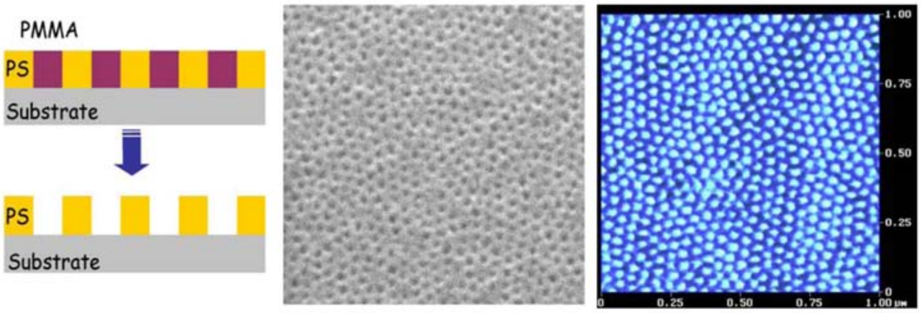


Fig. II.2.1: *Nanoporous thin film PS materials using P(S-b-MMA) diblock copolymers. (Left) Schematic describing the formation and removal of PMMA cylinders in a PS matrix. Plane-view SEM (center) and AFM (right) images of a nanoporous PS film onto Si and* Si_3N_4 *materials, respectively. The pores are about 20 (center) and 25nm (right) in diameter.*

B. Ge nanocrystals in high-k dielectrics obtained by low-energy ion-beam-synthesis

P. Dimitrakis, V. Ioannou-Sougleridis, P. Normand

The last few years, substantial research efforts have been placed on the fabrication of nanocrystals (NCs) in high-k dielectrics instead of SiO_2 materials to improve the performance of NC memories. Floating gate memory structures using high-k dielectrics as control and tunneling layers offer a thinner equivalent oxide thickness (EOT) without sacrificing charge retention. Band alignment of high-k dielectrics with Si results in a relatively narrow energy barrier and therefore, large tunneling currents across the tunneling layer are attainable at relatively low programming voltages. Part of our 2007-activities has been to explore the formation of Ge NCs in thin Al_2O_3 and Hf_2O layers using the low-energy ion-beam-synthesis (LE-IBS) technique and to evaluate the electrical performance of the resulting gate dielectrics.

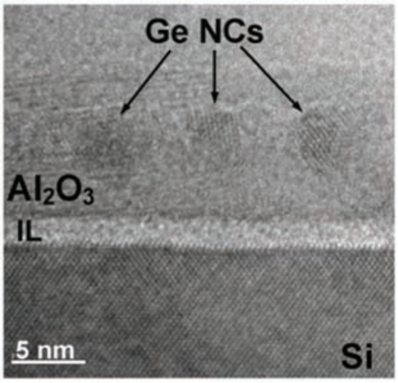


Fig. II.2.2: *High-resolution cross-section TEM image of Al_2O_3 materials with embedded Ge nanocrystals obtained by LE-IBS.*

For this purpose, 5 to 7nm thick Al_2O_3 layers were deposited on n-type Si wafers using the Atomic Layer Deposition (ALD) technique. The ALD-processed wafers were supplied by CambridgeNanotech (USA). Subsequently, the Al_2O_3 layers were implanted at FZR (Germany) with 1keV Ge atoms to doses of $5x10^{15}$ and $1.0x10^{16}cm^{-2}$. Then, a 10nm thick Al_2O_3 layer acting as control gate dielectric was deposited onto the implanted layers and the structures were thermal annealed for the purpose of Ge-NCs formation. The resulting structures were examined by transmission electron microscopy (CEMES/CNRS) and electrical characterization after fabrication of Al gate MIS capacitors.

In the case of 7nm-thick implanted-Al_2O_3 layers and thermal annealed at 800°C, high-resolution TEM (HRTEM) and Electron Energy Loss Spectroscopy (EELS) studies revealed the presence of Ge nanocrystals of 3-5 nm in diameter occupying the whole implanted Al_2O_3 layer and located at tunnel distances (1 to 5 nm) from the channel (see Fig. II.2.2). At this annealing temperature, presence of a 1nm-thick interfacial layer (IL, SiO_2-rich) between the Al_2O_3 layer and the Si substrate, as well as crystallization of the alumina matrix have been observed.

Capacitance-to-voltage characteristics of MIS capacitors with NCs revealed strong hysteresis in terms of flat-band voltage V_{fb} shift after application of gate-voltage round sweeps (see Fig. II.2.3). No significant hysteresis was detected for the unimplanted and the as-implanted samples. These results suggest that charge trapping and storage are related not only to the formation but also to the distribution of the Ge-NCs through the implanted/annealed Al_2O_3 layer. The effect of the annealing regime on the structural and electrical properties of Ge-NC-Al_2O_3 materials as well as the formation of Ge NCs into HfO_2 layers by LE-IBS are under investigation.

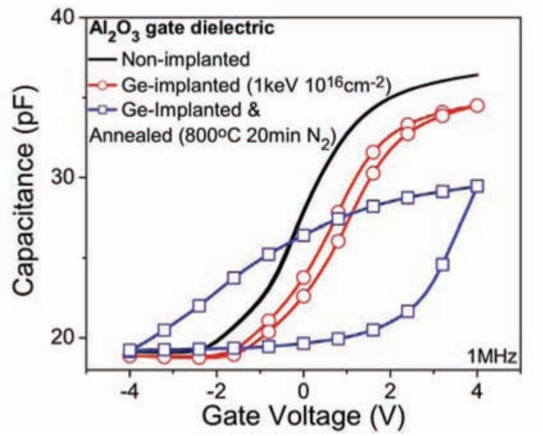


Fig. II.2.3: *High-frequency C-V curves after application of low gate voltage round sweeps.*

C. Channel edge effects in shallow-trench-isolated nanocrystal memories

P. Dimitrakis and P. Normand

Within the framework of the EU project NEON, prototype LE-IBS-Si-nanocrystal memory devices were fabricated at STMicroelectronics (IT) on 8-inch wafers using a process flow based on a 0.15μm Flash-EEPROM technology. The devices were isolated following a shallow-trench-isolation (STI) procedure. Capacitors and n-MOSFETs memory cells with gate lengths and widths ranging from 0.16 to 10 μm have been realized. Our electrical investigations stressed the following:

(a) Leakage currents occur at the channel isolation edges and lead to severe "subthreshold hump" effects in the transfer characteristics of 10x10μm^2 and 0.9x0.6μm^2 (WxL) devices. These leakage currents can be described in terms of parasitic transistors (FET_P) operating in parallel with the intrinsic transistor (FET_I) formed in the central part of the channel Fig.II.2.4). (b) Memory testing and threshold-voltage extraction according to the transconductance-change (TC) and constant-current methods, reveal that the parasitic transistors can be programmed or erased but exhibit memory characteristics different than that of the intrinsic transistor and thereby, can be treated as parasitic memories. Both erasing and programming are more efficient for FETI compared to FET_P. (c) No subthreshold "hump" is detected for the 0.16x0.3μm^2 devices. This is because the edge currents dominate the total drain current and the contribution of the intrinsic transistor is not immediately obvious; nevertheless the latter can be detected using the TC method (Fig. II.2.5). Further, transfer characteristics analysis and program/erase testing and comparison with capacitors and large channel area transistors reveal that the memory operation of these devices is FETP driven.

Although it is still difficult to draw safe conclusions regarding the origin of the parasitic memory effects in the devices reported here, our work suggests that the structural properties of the isolation regions affect dramatically the memory performance of the devices and may constitute a critical parameter in nanocrystal memory integration. Particular attention should be placed on STI architecture and device processing to overcome this technological concern.

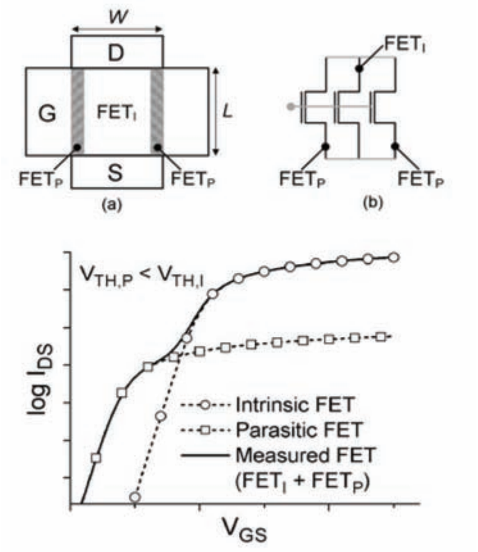


Fig. II.2.4: *Schematics describing (a) the channel edges where FET$_P$ are formed, (b) the equivalent circuit with FET$_I$ and FET$_P$, (c) the origin of the hump in the transfer characteristic of a MOSFET where FET$_P$ are active.*

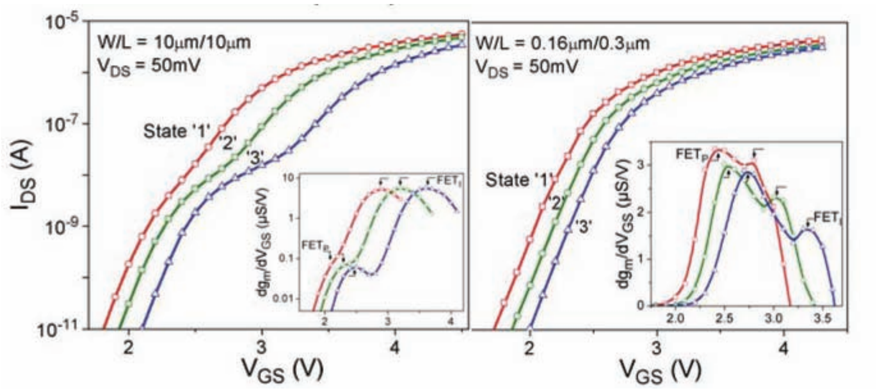


Fig. II.2.5: *Transfer characteristics of 10μm/10μm and 0.16μm/0.3μm Si-NC MOSFETs for four successive programming states. The corresponding dg_m/dV_{GS} vs V_{GS} plots are shown as insets.*

D. Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride

V. Ioannou-Sougleridis, V. Vamvakas, P. Dimitrakis, P. Normand

The use of thin tunnel SiO_2 layer (~2-3nm) in NCM technology allows high-speed operation at low voltages but addresses a critical issue for long retention times. If a thick oxide is used to enhance data retention, the advantage of high endurance and speed at reasonable voltages is lost rapidly. Different alternatives have been suggested for improving the performance of low-voltage NCMs without sacrificing charge retention. An interesting direction is to combine the advantages (low-voltage and high-speed) of NCM technology with those (long retention times, immunity to disturbance) of time-proven nitride-trap technology. Memory structures using SiO_2-Si_3N_4-SiO_2 (ONO) gate dielectric with nanocrystals embedded in the nitride layer are expected to gather together these advantages.

Our activities in this area started in 2005 with the realization of Si-NC ONO structures where Si-NCs were generated in the nitride layer by low-energy ion-beam-synthesis (LE-IBS). SiO_2-Si_3N_4 stacks were developed onto Si substrates and subsequently implanted at CEMES/CNRS with 1keV Si ions to doses ranging from $5x10^{15}$ to $1.5x10^{16}$ cm^{-2}. The thickness of the oxide and nitride layers was 2.8nm and 6.5nm, respectively. After the steps of post-implantation annealing and SiO_2 deposition, gate electrodes were fabricated by Al evaporation and patterning. In 2006, in-depth electrical and structural investigations were conducted at IMEL and CEMES. EFTEM examination revealed the presence of Si-NC and amorphous Si nanoparticles thin bands into the nitride layer for the $1.5x10^{16}$ (see Fig. II.2.6) and $1.0x10^{16}$ Si cm^{-2} samples, respectively. Electrical measurements indicate that significant changes compared to reference ONO stacks occur in the cases of the $1.0x10^{16}$ cm^{-2} and $1.5x10^{16}$ cm^{-2} samples, such as reduction of the onset voltage for electron and hole injection, reduction in electron storage ability and establishment of hole storage. Typical memory windows attainable under pulse operation and data retention characteristics at room temperature are shown in Fig. II.2.7-8. To date, our findings suggest that the Si-NC-ONO stacks are attractive for the further development of nitride storage memory cells.

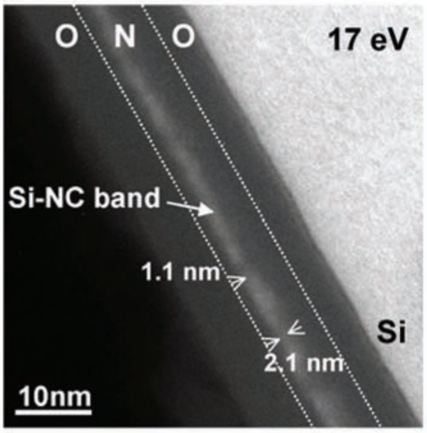


Figure II.2.6: *Cross-sectional EFTEM image (around 17eV) of a Si-NC ONO structure. The NCs were generated in the nitride layer by LE-IBS.*

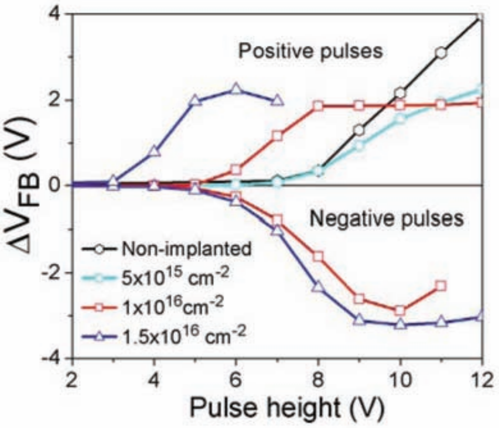


Fig. II.2.7: *Flat-band voltage shifts as a function of the gate pulse voltage of 100 ms duration for Si-implanted and unimplanted ONO stacks.*

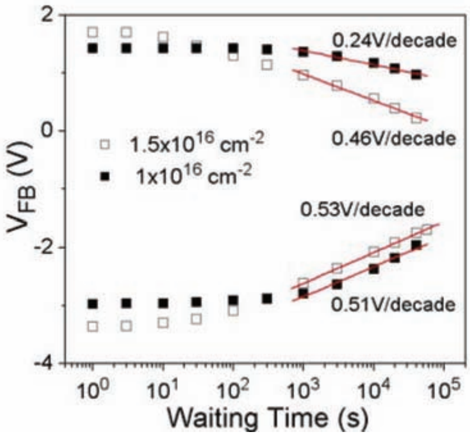


Fig. II.2.8: *Room-temperature retention characteristics of medium and high-dose Si-implanted ONO stacks.*

PROJECT OUTPUT in 2006

Publications in International Journals and Reviews

1. "Parasitic memory effects in shallow-trench-isolated nanocrystal memory devices", P. Dimitrakis and P. Normand, Solid-State Electronics, In Press, Corrected Proof, Available online 12 December 2006.
2. "Proton radiation tolerance of nanocrystal memories", E. Verrelli, I. Anastassiadis, D. Tsoukalas, M. Kokkoris, R. Vlastou, P. Dimitrakis and P. Normand, Physica E: Low-dimensional Systems and Nanostructures, In Press, Corrected Proof, Available online 16 December 2006.
3. "Metal nano-floating gate memory devices fabricated at low temperature", S. Koliopoulou, P. Dimitrakis, D. Goustouridis, P. Normand, C. Pearson, M.C. Petty, H. Radamson, D. Tsoukalas, Microelectronic Engineering 83, pp. 1563-1566 (2006).
4. "Oxidation of Si nanocrystals fabricated by ultralow-energy ion implantation in thin SiO2 layers", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, G. Ben Assayag, A. Claverie, M. Respaud, P. Dimitrakis, P. Normand, J. Appl. Phys. 99, 044302 (2006).

Conference Presentations

1. "Self-limited oxidation of Si nanocrystals elaborated by ultra-low implantation energy ion thin SiO2 layers", C. Bonafos, S. Schamm, H. Coffin, N. Cherkashin, G. Ben Assayag, A. Claverie, P. Dimitrakis, P. Normand, V. Paillard and M. Carrada, E-MRS 2006 Spring Meeting, Symposium C, Nice, France, May 29 – June 2, 2006.
2. "Proton radiation effects on nanocrystal nonvolatile memories", E. Verrelli, I. Anastassiadis, D. Tsoukalas, M. Kokkoris, R. Vlastou, P. Dimitrakis and P. Normand, Second European Conference on Radiation and its Effects on Components and Systems (RADECS 06), Athens, Greece September 27-29, 2006.

Invited Talks

1. "Materials Science Issues for the Fabrication of Nanocrystal Memory Devices by Ultra Low Energy Ion Implantation", A. Claverie, C. Bonafos, G.B. Assayag, S. Schamm, N. Cherkashin, V. Paillard, P. Dimitrakis, E. Kapetenakis, D. Tsoukalas, T. Muller, B. Schmidt, K.H. Heinig, M. Perego, M. Fanciulli, D. Mathiot, M. Carrada, P. Normand, Second International Conference on Diffusion in Solids and Liquids, Portugal, July 2006, Material Science Forum Vol. 258-260, pp 531-541.

Ph. D. thesis

1. P. Dimitrakis, Silicon nanocrystals for electronic memory devices, National Technical University of Athens, December 2006, Supervisor: P. Normand.

Diploma Theses

1. G. Niarchos, Fabrication and testing of MOS structures for memory applications, University of Athens, September 2006, Supervisor: P. Normand.
2. K. Parisiadis, Fabrication of nanostructures using P(S-b-MMA) diblock-copolymers, University of Ioannina, July 2006, Supervisor: P. Normand.

PROJECT II.3: MOLECULAR MATERIALS AS COMPONENTS OF ELECTRONIC DEVICES

Project leader: N. Glezos

Key researchers: N.Glezos, P.Argitis, P.Normand

Post Doctorals: A.Douvas, E.Makarona, E. Kapetanakis, D.Velessiotis, V. Chinnuswami

PhD candidates: G. Chaidogiannos, G.Tatakis

Funding:

- NMP STREP TASNANO, 1/1/2005-31/12/2007, Contract No 516865
- EU RTN project Uninanocups, 1/1/2004-31/12/2007, Contract No MRTN-CT- 2003-504233

Research orientation:

- To investigate the potential of molecular materials to be used as active components in molecular devices e.g. as switching or memory elements.
- to develop consistent evaluation methods based on the electronic transport properties at the nano- level for the characterization of single layered and few-layered systems.
- to produce physical parameters (film thickness, surface molecular density, contact potential) that could be cross-checked with other surface characterization methods
- To evaluate elements of the class of organic crystals as components of organic FETs
- To develop techniques for thin film deposition and characterization of molecular materials.

RESEARCH RESULTS

A. Organic/inorganic composite materials as components of nano-devices

A. Douvas, E.Makarona, E.Kapetanakis, N.Glezos, P.Argitis, P.Normand

a_1 *Synthesis and electrical characterisation of polyoxometallate layers*

A wide variety of organic molecules or metal nanoclusters have been proposed for molecular electronics applications in the past. Polyoxometalates (POMs) are inorganic metal-oxygen clusters that combine both the electron transport properties of the organic molecules with the charge confinement properties of the inorganic nanoclusters. POMs, especially the tungsten and molybdenum ones, have well-defined and stable structure consisted of clusters of coordination polyhedra MO_n that have a metal ion in their center and connect each other through common edges and apices. In previous work of our group, tungsten POMs were embedded into polymeric matrices using nano-distant planar electrodes, and conductivity peaks were evident even at room temperature conditions. During this year, the electric transport and charging properties of molecular monolayers consisted of POM anions and 1,12-diaminododecane (DD) cations, prepared with the layer-by-layer (LBL) self-assembly method were studied. It is shown that POM molecules act as electron traps and that tunneling dominates other transport mechanisms.

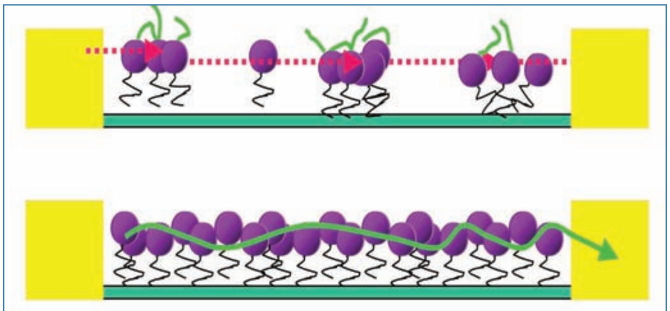


Fig. II.3.1. *Schematic diagram of APTES-POM films. The presence of diamine molecules on the top of the POM layer (purple spheres) results in creating clusters (top figure).*

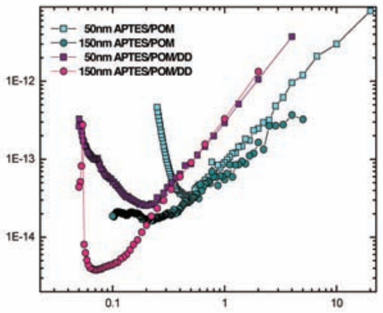


Fig. II.3.2. *I-V characterization and extraction of parameters from the F-N plots in the case of the various films. The transition point is affected by the presence of the diamine layer.*

During this year we studied the electronic transport properties of POM monolayers in planar structures using Au or Al electrodes on a silicon surface. Transprt is dominated by tunneling through the molecular layer. The presence of diamines result in a change of the film morphology which is detected as a change in the tunneling characteristic (figure II.3.2)

a_2 *C-MOS capacitor devices containing molecular monolayers*

Novel structures using C-MS compatible processes were fabricated. These structures contain patterned molecular layers. The aim is to selectively charge the molecular layer and thus create a molecular memory module. These structures were extensively studied using I-V and CV spectroscopy. The gate / substrate properties are under investigation. It is desirable to charge the system only from one side (substrate).

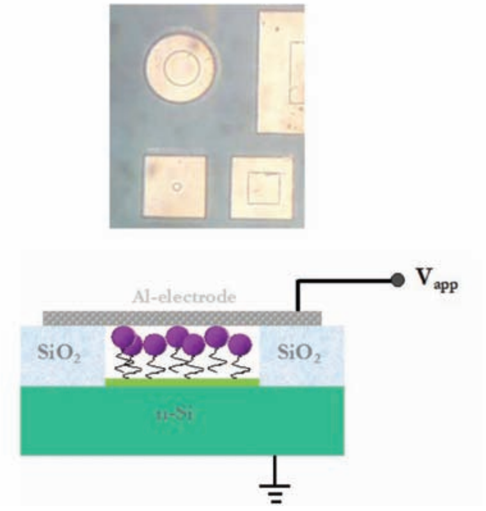


Fig. II.3.3: *Schematic of the fabricated capacitors which encapsulate the molecular layer.*

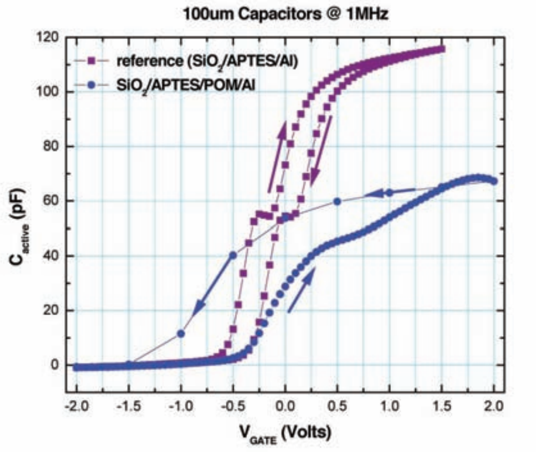


Fig. II.3.4: *CV behaviour of the molecular films.*

B. Transport properties of Cyclodextrin/Au nanoparticle host/guest systems

D. Maffeo[1], V. Chinnuswamy, D. Velessiotis, N.Glezos, K.Yannakopoulou[1], I.M.Mavridis[1]

[1]Institute of Physical Chemistry, NCSR "Demokritos"

The aim of this work is to fabricate nanodevices based on the transport properties of composite organic/Au nanoparticle systems. In this case, cyclodextrin derivatives bearing long aliphatic sulfide substituents were synthesized at the institute of Physical Chemistry. The derivatives feature (a) not-easily oxidizable sulfides (as opposed to thiol-groups which are prone to oxidation to sulfoxides or even sulfones), which offer seven points of attachment to the Au surface and (b) the -S- groups are connected to the cyclodextrin ring through a 10-carbon spacer, providing ample flexibility for structural organization during the deposition on the gold surface. Attachment of these molecules on Au surfaces was confirmed by RAIRS.

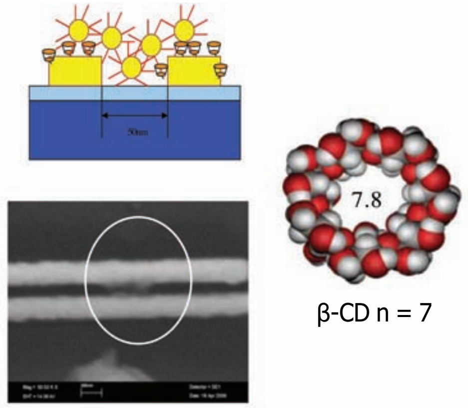


***Fig. II.3.5:** Cyclodextrin nanodevice. The cyclodextrines are accumulated in the electrode gap.*

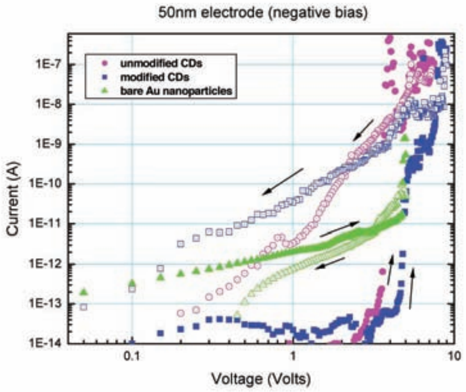


***Fig. II.3.6:** Memory effect (blue line) resulting from tunnelling through modified cyclodextrines*

The resulting system consisted of the two nanoelectrodes (50nm distance 5μm length) and an accumulation of Au nanoparticles bridged by the cyclodextrins properly functionalised for attachment on gold nanoelectrodes. In the case of current measurements the Au nanoparticles act as donors/acceptors of electrons with different potential in each case. The system is reversibly charged/uncharged (fig. II.3.6) showing instability when the applied voltage is decreased. In the optimised case only one pair of molecules are coupled to one gold nanoparticle and the nanoelectrodes.

The cylodextrine functionalised gold surfaces were also studied using STM imaging and I-V spectroscopy. The morphology of the film was demonstrated. Small clusters of very few atoms are created on the surface. These clusters are organised in larger stripes. The tunnelling barrier height decreases due to the presence of the molecular layer.

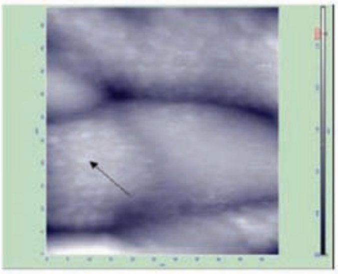


Fig. II.3.7: *Cyclodextrine arrangement on a gold surface using STM. The nanometer size spots correspond to the accumulation of a small number of molecules.*

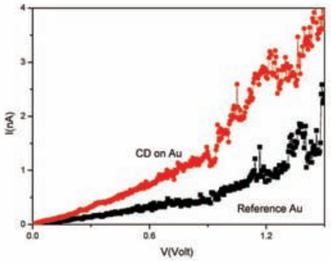


Fig. II.3.8: *STM spectroscopy of cyclodextrines on gold.*

C. Evaluation of organic crystals for OTFT applications

G.Chaidogiannos, N.Glezos, S. Kennou[2], F. Petraki[2], S. Nespurek[3]

[1]Institute of Physical Chemistry, NCSR "Demokritos"

[2]Department of Chemical Engineering, University of Patras

[3]Institute of Macromolecular Chemistry, Academy of Sciences of the Czech Republic

We investigate the class of metal phthalocyanine salts (MePCs) and metal phthalocyanine sulfonate sodium salts (MeS_xPCs) as candidates for p-type channels in organic transistors. Both kinds have the advantage of chemical and thermal stability (stable up to 400°C, easily evaporated). The field mobilities of MePCs in transistor structures are in the range of 0.02 cm^2/V.s (for CuPC). Recently, a mobility value of 1 cm^2/V.s in the case of CuPC single crystals was reported. Furthermore, MePCs are interesting for electronic applications such as chemical sensors and solar cells]. MeSxPCs are selected because of their enhanced solubility compared to their non-sulfonated counterparts, and were either synthesized (Me=Ni, Co, Zn or Al) by the Czech partner, or purchased by Aldrich Co (Me=Cu).

The comparison between the MePCs studied was based on their electric behavior depending on a) the method of deposition, b) the type of metal and c) the presence of pendant groups. The objective is to select the type of material and the film preparation process with the optimal performance. Preliminary tests for Al(OH)PC$(SO_3Na)_x$ based transistors have given promising results.

On the other hand, metal phthalocyanine sulfonate sodium salts, are innovative materials, which can be used to construct OTFTs with much less effort. The processes are much simpler and the mobilities obtained are much higher. In that case the active layer is prepared by spin coating at room temperature, using the MeSxPC solutions. Afterwards, the samples are dried at elevated temperature (50°C) for 20 minutes.

The first system studied was NiPC as a reference. Fig. II.3.9(a) shows a typical set of characteristics for a device with a 50nm active layer. The field effect mobility is 10^{-5} cm^2/V.sec, a value that agrees with previously published results and is acceptable for the applications to which those materials address.

Higher mobility values are obtained in the case of metal phthalocyanine sulfonate sodium salts. The drain source conductivity increases with negative gate bias indicating typical p-type conductivity. OFETs with MeS_xPCs as the active channel cannot be fabricated by evaporation, since the material tends to burn out before it evaporates. Results for the whole class has been investigated.

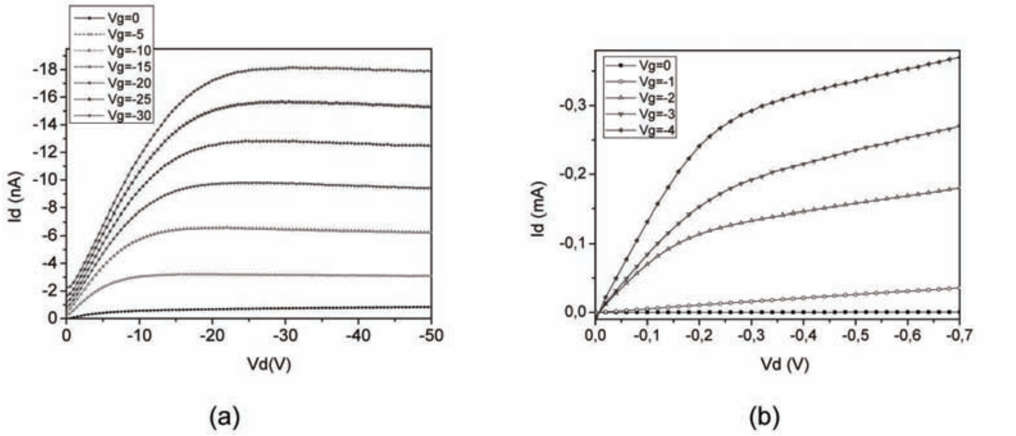


Fig.II.3.9: *Dependence of drain current on the drain voltage of an OFET with 50nm organic layer, W/L ratio of 23275 and 82nm thick SiO_2 oxide dielectric: (a) NiPC deposited at a substrate temperature 100°C. The calculated field effect mobility is 10^{-5} $cm^2/V.sec$. (b) $NiS_{2.4}PC$ layer, deposited by spin-coating and annealed at 50°C. The calculated field effect mobility is 1.08 $cm^2/V.sec$. All device characteristics are measured in room ambient.*

PROJECT OUTPUT in 2006

Publications in International Journals

1. "Electrical characterization of molecular monolayers containing tungsten polyoxometalates", Glezos N, Douvas AM, Argitis P, et al., Microelectron. Eng. 83 (4-9): 1757-1760 Apr-Sep. 2006
2. "Electron-beam lithography simulation for the fabrication of EUV masks", Patsis, G.P., Tsikrikas, N., Raptis, I., Glezos, N., Microelectronic Engineering 83 (4-9 SPEC. ISS.), pp. 1148-1151 (2006)

Papers in Conference Proceedings

1. "Single-Component Nickel-1,2-Dithiolene Complexes, Candidate Semiconductors For Field-Effect Transistors", G.C.Papavassiliou, G.C.Anyfantis, B.R.Steele, A.Terzis, C.P.Raptopoulou, G.Tatakis, G.Chaidogiannos, N.Glezos, Y.F.Weng, H.Yoshino, and K.Murata, International Conference on Science and Technology of Synthetic Metals (2006), Dublin, Ireland
2. "Organic transistors using metal phthalocyanines", G.Chaidogiannos, F.Petraki, N.Glezos, S.Kennou, S.Nešpůrek XXII Greek Solid State and Material Science Conference (2006), Patras, Greece

PhD Thesis

1. D.Velessiotis, Microelectronic nanostructures and nanodevices based on polyoxometalates, Information Faculty, University of Athens, December 2006

Diploma Theses

1. M.Kalonakis, Molecular Transistors using organic crystals, SEMFE, NTUA, November 2006
2. C.Livitatsanos, Electrical properties of molecular devices based on organic/inorganic materials, SEMFE, NTUA, November 2006

Research Programme III

SENSORS & MEMS

PROJECT III.1: POROUS SILICON TECHNOLOGY and APPLICATIONS

Project Leader: A. G. Nassiopoulou

Other key researcher: H. Contopanagos, G. Kaltsas

Post-doctoral scientist: D. Pagonis

Phd students: F. Zacharatos, A. Petropoulos

Funding:

- EU Marie Curie/ "RF on porous", re-integration grant, Contract No 016142, 29/7/2005-28/7/2007
- Contract with the National Research Agency-Cyprus, Photothermal analysis, 1/7/2004-30/6/2006
- Contract with the company Unilever UK, Flow system for Unilever, 1/12/2005-31/5/2007
- Contract with the company ST Microelectronics SA France, RF-on-porous, 30/7/2005-30/7/2008

Research orientation:

- Porous silicon material development: mesoporous and macroporous silicon
- Development of silicon micromachining technologies using porous silicon
- Application in flow sensors, accelerometers, microfluidic devices and on-chip integration of RF components.

a) *Porous silicon technology for sensors*

A big effort has been devoted the last years at IMEL in developing materials and enabling technologies for application in sensors. One such material platform with important potential for applications in different sensor devices, microfluidics, lab-on-chip, integration of passives on silicon etc. is porous silicon technology.

Either nanostructured mesoporous or macroporous silicon are grown at IMEL. Mesoporous silicon is very appropriate for use as micro-plate for local thermal or electrical (dc, RF) isolation on a silicon substrate. Macroporous silicon is developed for use in photonics, via technology, device cooling and particle filtering.

Different technologies based on porous silicon are available at IMEL, including:

- Proprietary micromachining techniques based on the use of porous silicon as a sacrificial layer for the fabrication of free standing membranes, bridges and cantilevers on a silicon substrate
- Technologies using porous silicon for local thermal or RF isolation on a silicon wafer, or using porous silicon as a matrix for the deposition of catalytic materials for use in chemical sensors

b) *RF isolation by porous silicon micro-plates on a silicon substrate*

This activity is more recent at IMEL. The overall objective is:

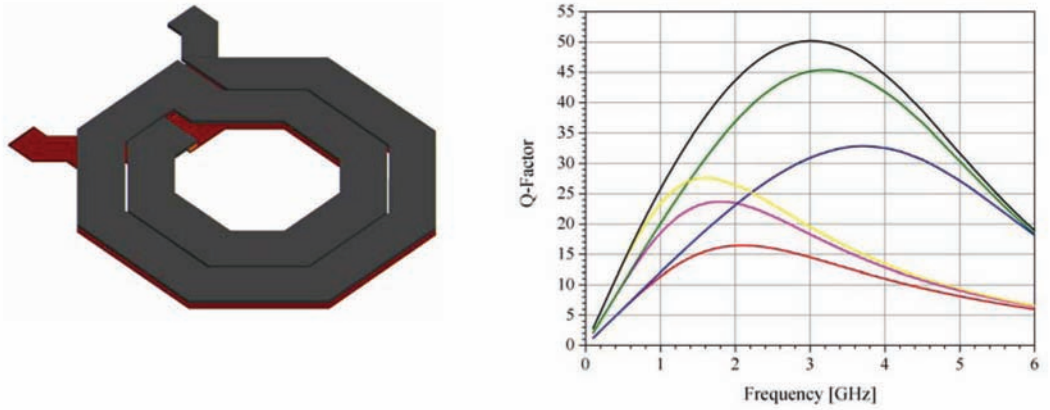
- to explore and extend porous silicon technology into the domain of CMOS-compatible integrated RF systems for use in systems-on-chip and
- to improve the performance of currently integrated analog CMOS components by above technology transfer and related optimization of design methodologies.

RESEARCH RESULTS

A. Integrated inductors on Porous Silicon in CMOS-compatible processes

H. Contopanagos, D. Pagonis and A. G. Nassiopoulou

Radio-frequency (RF) components such as inductors, capacitors, filters, transformers and other resonators, integrated on-chip, are essential building blocks of all analog radio frequency integrated circuits (RFICs) and their performance at current and future CMOS processes is a major bottleneck to successful system integration, especially for single-chip radios at high frequencies. It is clear that fully on-chip inductors in a CMOS-compatible process substantially improving the current art would create an important competitive advantage in the overall performance/cost ratio compared to hybrid technologies. In this work we explored the use of porous silicon as a compact micro-plate with low RF losses, grown locally on the silicon substrate by electrochemistry, as a way to implement significantly higher-Q RF inductors on a standard CMOS technology. We have shown that using a 50µm-thick porous Si RF micro-plate on standard CMOS technology, respecting corresponding metallization foundry rules, increases the Q-factors of the inductors as follows: On 0.18µm CMOS (Al metallization), the Q-factor enhancement is 50%-60%. On 0.13µm CMOS and smaller-scale nodes (Cu metallization) the enhancement is about 100%. Using an in-home CMOS-compatible process allowing 2 metal layers, the corresponding maximum Q-factors for the same optimized metallization is 17 and 34 respectively. When a standard CMOS metal stack of 6 Cu layers is used, the maximum Q-factor reaches 50, which is comparable with the performance of much larger off-chip inductors. Of equal importance, the frequency shape of the Q-factors with porous Si benefits the higher wireless communications bands (Bluetooth-WLAN). Currently, we are working on RF electrical characterization of porous Si and we fabricate the corresponding inductors.



(a) (b)

Fig. III.1.1: *a) Optimized 2-metal inductor layout: Grey = M2 (top metal); Brown = M1 (bottom metal closest to Si). b) Q-factors of optimized inductors of the same inductance and self-resonant frequencies for 0.13µm CMOS: Blue/Red = 2 metals with/without porous Si; Green/Magenda = 4 metals with/without porous Si; Black/Yellow = 6 metals with/without porous Si.*

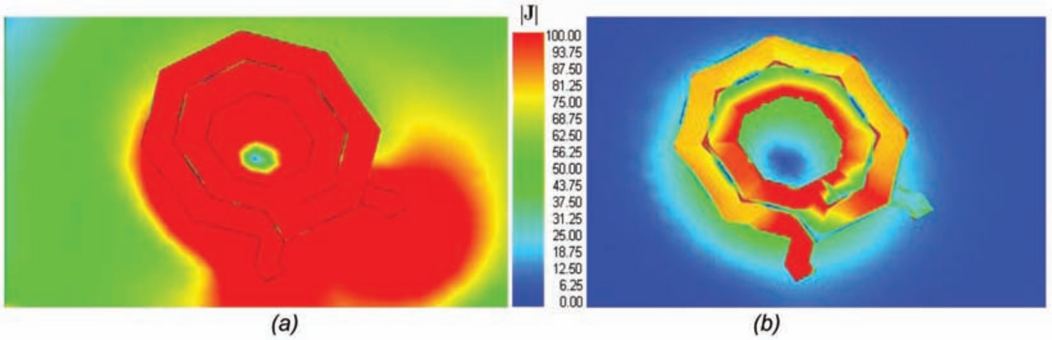


Fig. III.1.2: *Lateral current density magnitude distribution 50μm underneath M1: a) Without porous Si and b) with porous Si.*

B. Confined macroporous silicon membranes on pre-defined areas on the Si substrate

D. N. Pagonis and A. G. Nassiopoulou

In this work we investigated the formation of confined macroporous silicon membranes on pre-defined areas on the silicon substrate. Two different cases were considered: a) membranes supported by the silicon substrate and b) membranes suspended over a cavity on Si. The confined areas were defined lithographically and porous silicon formation took place at mask openings. The main difficulty to overcome was to avoid trenching and silicon over-etching at mask borders. A detailed study was undertaken to find an optimum masking material in order to avoid the trench formation at the borders of the lithographically defined areas. An appropriate masking technology was developed and used to fabricate a) single macroporous and b) bilayers of macroporous over mesoporous silicon. In the second case, by selectively removing the mesoporous layer, suspended confined macroporous silicon membranes over a cavity on the silicon substrate were fabricated (figure III.1.3).

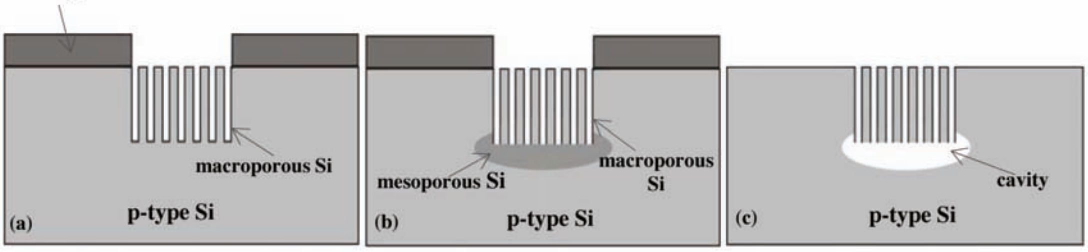


Fig.III.1.3: *Scematic representation for the formation process of free-standing macroporous membranes over a cavity; a) Formation of a confined macroporous silicon membrane through a lithographic mask; b) Formation of mesoporous Si underneath the macroporous layer; c) Mesoporous Si dissolution and cavity formation - Mask dissolution*

The new masking technique is based on the creation of n-type silicon areas by ion implantation. Appropriate experiments were carried out using the developed technology. Typical obtained results are presented in figures III.1.4a & III.1.4b below. Macroporous silicon membranes have been successfully formed locally only at the defined geometry by the n-type areas. There are no trenches created at the sides of the macroporous silicon membrane and there is no surface etching at the borders of the n-type area. The developed process is fully compatible with silicon processing for IC fabrication. The obtained results are promising and show an important potential for the fabrication of useful structures for different applications, as for example lab-on-chip and drug delivery systems. Although the technique needs further improvement and optimization for the formation of deeper macroporous layers, its potential for the formation of supported and free-standing macroporous silicon membranes on p-type wafers has been demonstrated.

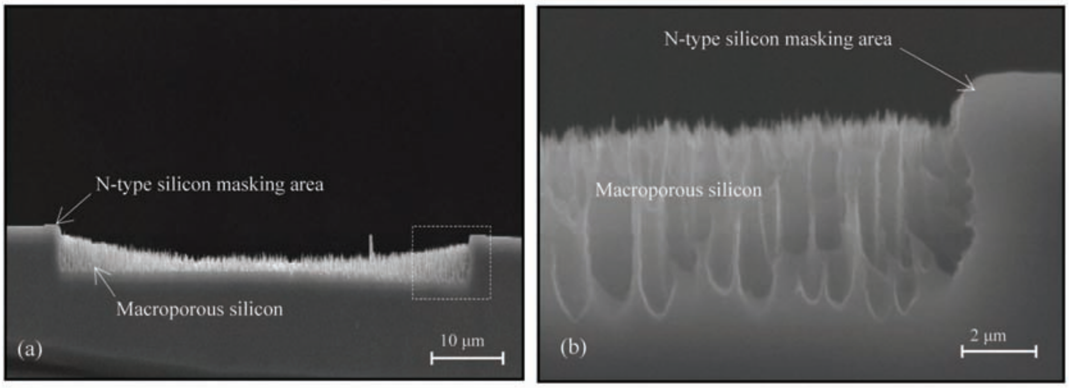


Fig. III.1.4: *SEM images of the cross-section of a confined macroporous silicon membrane. The masking material used was n-type Si created through P implantation. The trenches at the sides of the membrane are not formed. The area selected by the square in picture (a) is magnified in (b).*

C. Microfluidic flow sensor based on porous silicon technology

D. N. Pagonis, A. Petropoulos, G. Kaltsas, A. Tserepi and A. G. Nassiopoulou

This work concerns the fabrication, modelling and testing of a novel microfluidic flow sensor based on a microchannel capped with a porous silicon membrane, on top of which the sensor active elements are integrated. The microchannel is formed through a two-step anodization process. In the first step a mesoporous silicon layer is formed on a lithographically defined area, while in the second step a channel is formed underneath the porous layer by electropolishing. The channel is buried into bulk silicon and capped with a free-standing porous silicon layer, which is co-planar with the Si substrate. The developed technology shows important advantages compared to other existing techniques, which are: a) the simplicity and low cost of the process (formation of a self-sealed, buried microchannel in a single two-step electrochemical process) and b) the compatibility of the process with integrated circuit fabrication processing, which allows integration of the device on the same chip with silicon electronics.

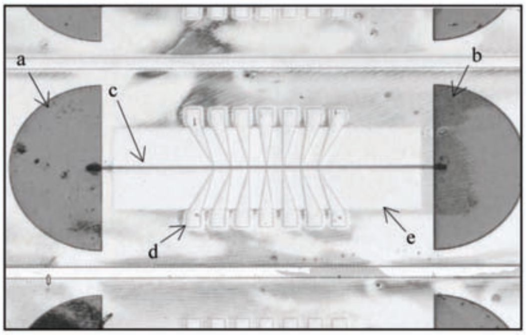


Fig. III.1.5: *Top-view optical picture of the formed microfluidic sensor, where we identify the inlet (a) and outlet (b) semi-circular reservoirs of the device, the buried microchannel (c) and the integrated sensing elements (d). The passivation layer on top of the active area of the device is also seen (e).*

Investigation of the device operation has been performed through appropriate simulations. Experimental testing of the prototype has been performed, after mounting the device in an appropriate package.

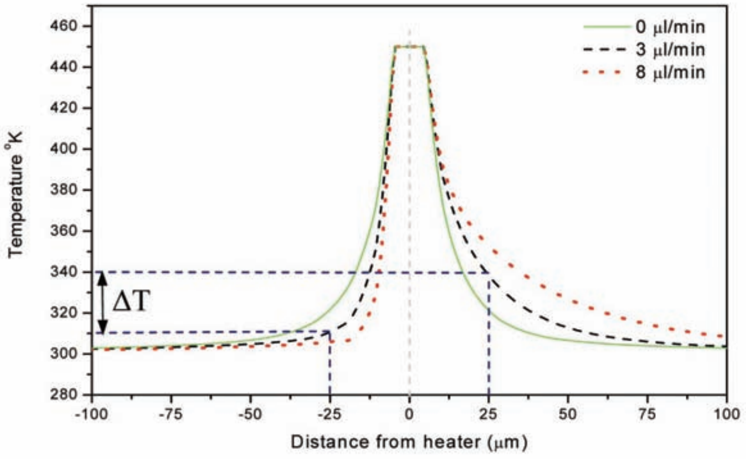


Fig. III.1.6: *Typical simulation results of the temperature distribution on the porous silicon capping layer of the microchannel. A symmetrical distribution is obtained with respect to the centre of the heater (dashed vertical line), when no flow is assumed, as expected. On the contrary, under flow, a significant asymmetry is observed due to convective heat transfer. The resulting temperature difference (ΔT) between two symmetrical points, situated 25 μm away from the heater has been indicated for a flow of 3 μL/min. The larger the flow rate is, the greater is the departure from symmetry.*

In order to demonstrate the functionality of the device, liquid was pumped into the inlet of the device at various flow rates from 2 μl/min up to 60 μl/min, while optical pictures under a microscope were taken. The liquid debouched successfully only through the outlet of the device, thus, the microchannel is empty from any remnants which could have been created from the electropolishing stage of the microchannel formation process, while the capping layer has sufficient mechanical stability to withstand the pressure induced by the flow of the liquid. Further experimental characterization of the device operation is in progress.

D. Copper wires within macroporous Silicon layers

F. Zacharatos and A. G. Nassiopoulou

In the present work a novel technique concerning the development of copper wires in a macroporous silicon template is demonstrated. Electrochemistry has been utilized for both the fabrication of the macroporous silicon films and the copper deposition inside the pores.

The starting materials in this investigation were p-type, 6-8Ω.cm silicon wafers. Their surface was pre-patterned properly, since the resulting structure was intended to have a specific arrangement. The pre-patterning process includes photo-lithographic as well as silicon wet etching steps. The result of this procedure is the formation of pore initiation pits that resemble inverted pyramids and form regular arrays on the substrate. The succeeding electrochemical anodization lead to the formation of regularly ordered arrays of pores with a diameter of 4-8μm (fig. III.1.7a) The thickness of the porous layer ranged from 30 to 120μm (fig. III.1.7b). By optimizing the electrochemical conditions, pores with even greater aspect ratios can be achieved.

The successful fabrication of the macropore arrays is followed by a thin thermal oxide development and a second electrochemical process. During this procedure, whose duration may exceed 120 min, copper particles are forced to deposit on the pore walls (fig. III.1.8a) and inside the macroporous film, until the pores are completely filled. The efficiency of the electrolytic solution is very sensitive in terms of composition and pH. The implementation of appropriate conditions followed by annealing, result in the development of homogeneous and consistent 50μm long copper wires (fig III.1.8b).

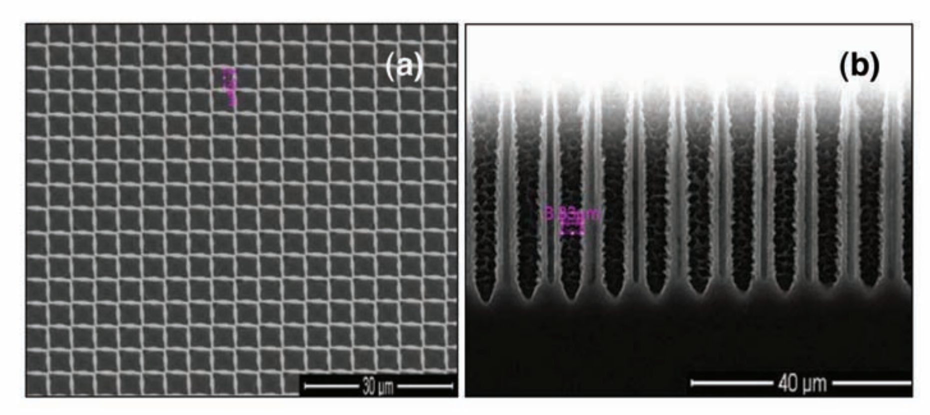


Fig. III.1.7: *SEM image of a typical ordered Macroporous Silicon layer formed on a p-type Si wafer. In (a) a top and in (b) a cross-sectional view of a sample with 50μm long pores are shown.*

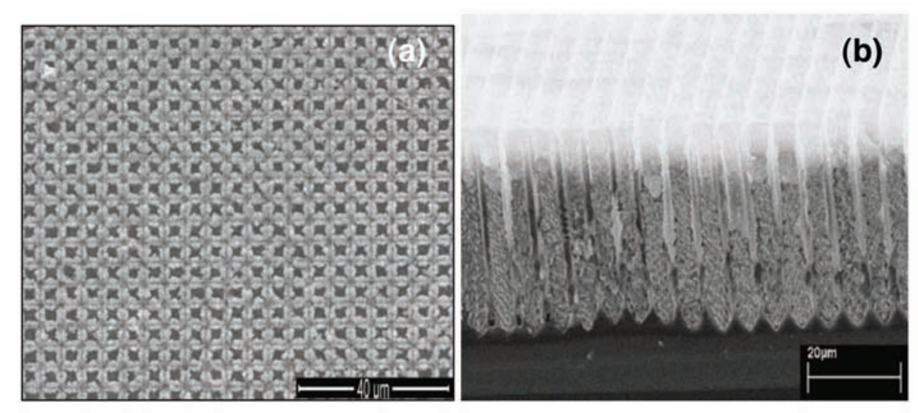


Fig. III.1.8: *SEM image of the samples after Cu deposition. (a) On the surface copper particles cover the pore walls (b) In cross-section, 50μm long copper wires are observed.*

PROJECT OUTPUT in 2006

Publication in Refereed Journals

1. "Design and simulation of integrated inductors on porous silicon in CMOS-compatible processes", H. Conopanagos and A. G. Nassiopoulou, Sol. St. Electronics, vol. 50 (7-8) 1283 (2006)
2. "Free-standing macroporous silicon membranes over a large cavity for filtering and lab-on-chip applications", D. N. Pagonis and A. G. Nassiopoulou, Microelectronic Engin. 83, 1421–1425 (2006)

Papers in Conference Proceedings

1. "Porous silicon for sensors and on-chip integration of RF components", A. G. Nassiopoulou (invited paper), Proceedings of the 4th International Conference on Microelectronics, Devices and Materials, Slovenia 13-15 September 2006, p. 33
2. "Integrated inductors on porous silicon", H. Contopanagos, A. G. Nassiopoulou, Proceedings of the 5th International Conference on Porous Semiconductors-Science and Technology (PSST), Sitges-Barcelona, 12-17 March, 2006
3. "Local formation of suspended macroporous Si layers on a Si substrate", D.N. Pagonis, A.G. Nassiopoulou, Proceedings of the 5th International Conference on Porous Semiconductors-Science and Technology (PSST), Sitges-Barcelona, 12-17 March, 2006
4. "Novel microfluidic flow sensor fabricated using porous silicon technology", D.N. Pagonis, A. Petropoulos, G. Kaltsas, A.G. Nassiopoulou, A. Tserepi, Proceedings of the 5th International Conference on Porous Semiconductors-Science and Technology (PSST), Sitges-Barcelona, 12-17 March, 2006
5. "A silicon integrated thermal liquid flow sensor on porous silicon micro-hotplate", D. N. Pagonis, G. Kaltsas and A. G. Nassiopoulou, Proceedings of the 20th Eurosensors Conference, Göteborg, Sweden, 17-20 September 2006

Conference Presentations

1. "Copper wire fabrication in macroporous Silicon templates", F. Zacharatos and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006
2. "Fabrication of SiO2 quantum dots on Si Substrate through porous aloumina mask", V. Gianneta, M. Kokonou and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006
3. "Porous anodic aloumina on Si as a template for Au nanowires fabrication", V. Gianneta and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006
4. "A novel microfabrication technology for plastic sensors formation", I. K. Tsougeni, G. Kaltsas, A. Petropoulos, P. Asimakopoulos, D. N. Pagonis and A. G. Nasiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006
5. "Integrated microflow sensor based on porous silicon technology", D. N. Pagonis,A. Petropoulos,G. Kaltsas and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006

Invited Talks

1. "Porous silicon for on-chip integration", A. G. Nassiopoulou (Tutorial), PSST-2006, Barcelona-Spain, 12-17 March 2006
2. "Porous silicon for sensors and on-chip integration of RF components", A. G. Nassiopoulou (Invited Talk), 42th International Conference on Microelectronics, Devices and Materials and Workshop on MEMs, NEMs, September 13-15, 2006, Slovenia

Organisation of Conferences, Symposia, Workshops

1. PSST - 5th International Conference on Porous Semiconductors-Science and Technology, Sitges-Barcelona, 12-17 March, 2006, Chairpersons: V. Parkhutik, L. Canham, A. G. Nassiopoulou, M. Sailor, Edition of Proceedings, Special issue of Physica Status Solidi, Physica Status Solidi

Patent filing

1. "Low power silicon thermal sensors and microfluidic devices based on the use of porous silicon sealed air cavity or microchannel technology", PCT patent, International publication, No W003/062134, Inter. Publ. date: 31/7/2003, Filing in USA, Japan Europe, China

DISTINCTION

Cover page of Physica Status Solidi, May 2007

Cover picture story pss (a) 204-5: **Integrated Inductors on Porous Silicon**

The cover picture illustrates the effective use of a thick porous silicon layer as an integrated micro-plate for RF isolation on a silicon substrate, proposed by Harry Contopanagos and Androula Nassiopoulou in their Original Paper [1] in the current issue. What is plotted is the magnitude of the current distribution on the metallization and on a screen 50mm underneath the bottom oxide layer of a 2-metal integrated CMOS-compatible inductor on bulk silicon (left) and on a 50 Ìm thick porous silicon layer (right) for a frequency of 2.5 GHz.

[1] H. Contopanagos and A. Nassiopoulou, phys. Stat. sol. (a) 204 No5, 1454-1458 (2007)

PROJECT III.2: MECHANICAL AND CHEMICAL SENSORS

Key Researchers: C. Tsamis, I. Raptis, P. Normand

Other Collaborating researchers: A. Tserepi

Post-doctoral scientists: S. Chatzandroulis, D. Goustouridis, E. Makarona, F. Farmakis

Phd candidate: R. Triantafyllopoulou

Objectives:

- Development of micromachining processes for the realization of novel chemical and mechanical sensors
- Development of low power silicon sensors based on new materials and new processes
- Design, fabrication and testing of microsystems using silicon sensors
- Realization of sensors for specific industrial applications with emphasis on medical, food and automotive fields

Funding:

- EU - IST-FP6-STREP-027333 Micro2DNA, *"Integrated polymer-based micro fluidic micro system for DNA extraction, amplification, and silicon-based detection"*, P. Normand
- GSRT – Technogenesis no 67, *"Miniature sensor for the control dangerous tire pressure and malfunction of ball bearings and breaks"*
- EU, IST, IP, GOODFOOD, *"Food Safety and Quality Monitoring with Microsystems"*, contract No. 508774, C. Tsamis
- GSRT Greece-Italy bilateral cooperation *"Fabrication and characterization of an array of transparent conductive thin film polymeric composite as multiparametric sensitive layers for a new e-nose"*, D. Goustouridis
- GSRT-PENED 03ED630, *"Micromachined chemical sensors for controlling food safety and quality"*, C. Tsamis
- GSRT- ENTER 05EP032, *"Development of MOSFET type chemical sensors for wireless sensor networks"*, C. Tsamis

RESEARCH in 2006

Research in 2006 focused in the following:
a) Alternative micro-hotplate design for low power metal-oxide (MOX) sensor arrays
b) Electronic ASIC for MOX Chemical Sensors
c) Polymer based chemical sensors
d) Capacitive Type Sensors
e) Suspended Cantilevers for Electromagnetic Energy Harvesters

RESEARCH RESULTS

A. Low power Metal-Oxide (MOX) Chemical Sensors based on Porous Silicon Micro-hotplates

R. Triantafyllopoulou, C. Tsamis, S. Chatzandroulis, F. Farmakis, and A. Tserepi

Solid state gas sensors based on SnO_2, are widely used in both indoor and outdoor applications, due to their low cost and high sensitivity. The sensing mechanism of these sensors is based on the changes of the conductivity of the SnO_2 sensitive layer, which is deposited between two electrodes, due to the adsorption of reducing or oxidizing agents onto its surface. One disadvantage of this type of sensors is that their operating temperature is in the range of 300-400°C, which results in a considerable amount of power being consumed on an embedded heater. In order to reduce the power requirements of the sensor, the sensitive SnO_2 layer has been integrated on Porous Silicon Micro-hotplates, developed in the previous years. Porous Silicon provides improved thermal isolation, thus reducing heat dissipation to the substrate (Fig III.2.1).

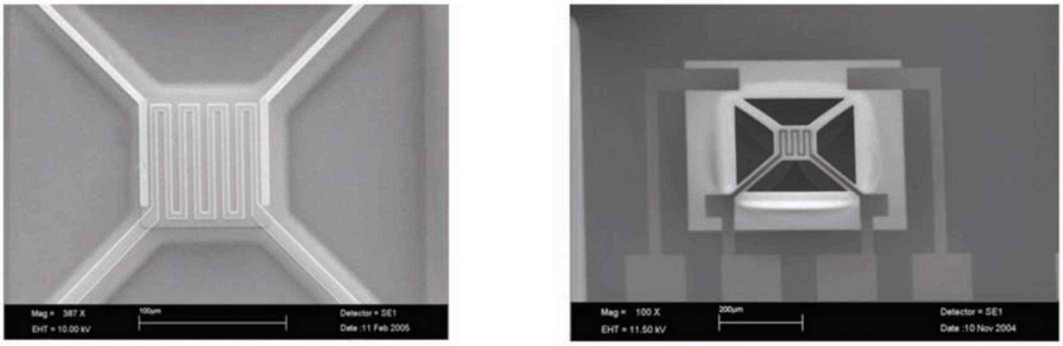


Fig. III.2.1: *(a) SEM image of a not-released PS micro-hotplate. We can see the sensitive material deposited of the membrane. (b) SEM image of a released PS micro-hotplate, with integrated heater and electrodes*

During this year, we have fabricated gas sensor devices for food safety and quality applications as well as for environmental monitoring. The response of the SnO_2 gas sensors was measured for the various gases (NH_3, CO and NO) and gas concentrations (50-500 ppm). Analysis was performed in isothermal mode (Fig. III.2.2(a)), by keeping constant the micro-hotplate temperature and in pulsed temperature mode (Fig. III.2.2(b)), by applying voltages pulses to the heater. In this case, the sensitivity and selectivity of the sensors was estimated as a function of the total shape of the pulse cycle, the duration of the pulses and the temperatures of the "hot" and the "cold" part of the measuring cycle. Very good sensitivity has been achieved with very low power consumption.

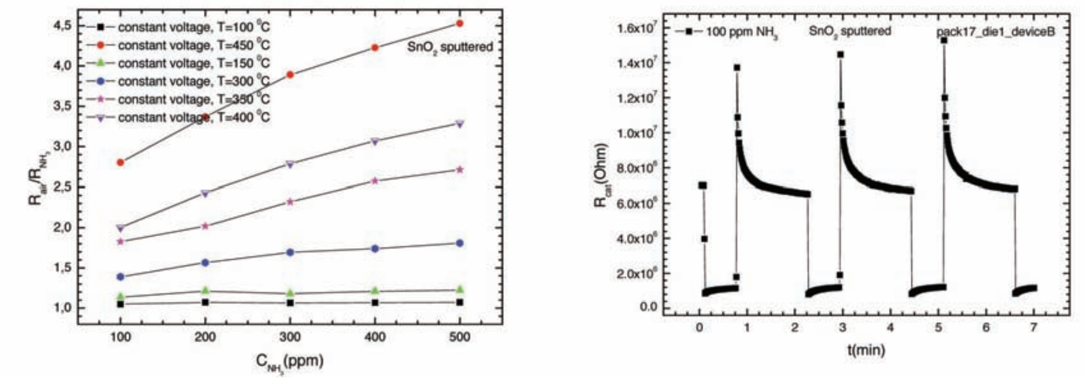


Fig. III.2.2: *(a) Sensor sensitivity as a function of the NH_3 concentration for temperatures between 100-450 °C, (b) Sensor resistance in pulsed operation mode for 100 ppm NH_3 and T_{hot}=350 °C, t_{hot}=40s and T_{cold}=100 °C, t_{cold}=90s.*

For more information please contact Dr. C. Tsamis (e-mail: ctsamis@imel.demokritos.gr)

B. Control and Electronics for MOX Chemical Sensors

P. Robogiannakis, S. Chatzandroulis and C.Tsamis

The correct operation of metal oxide (MOX) sensors requires that precise control over the operating temperature of the device is exercised simultaneously with the read-out of the chemically sensitive resistance. To this end, an electronic ASIC (Fig. III.2.3) has been developed able to interface a quad gas sensor array to a microcontroller and thereon to a PC or E-nose system. The chip contains in a single IC all the necessary analog electronics to operate four MOX sensors while the control logic will be implemented on the microcontroller (fig III.2.4). The ASIC has successfully been implemented in a single-poly, double-metal, 0.7um CMOS process (fig III.2.3) and first measured results are in agreement with simulated values. Provision has been taken for both polysilicon and Pt heater control.

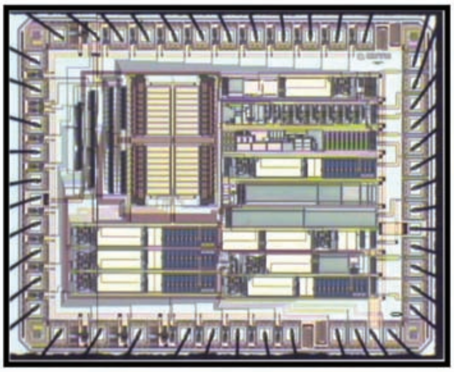


Fig. III.2.3.: *Fabricated ASIC chip*

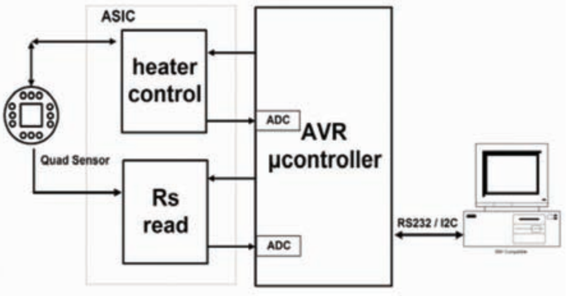


Fig. III.2.4: *Schematic of the MOX electronic control system.*

After testing of the basic functions of heater control and sensitive resistance readout of the gas sensor interface ASIC were tested, the chip was used with an actual commercial MOX sensor from Microsens. The sensor operates on a steady heater voltage of 1.68V (isothermal mode) provided from the ASIC. Changes in the sensitive resistance were sensed and transformed into a voltage signal (Vout). In Fig. III.2.5, measurements during exposure of the sensor to 220 ppm of NO gas are depicted.

Subsequently a PCB for the MOX control board which contains the ASIC and a microcontroller was designed. The completed PCB for the control and read out of a four MOX sensor array is depicted in Fig. III.2.6. The development of the firmware is underway and the microcontroller is able to transmit sensor values through the RS-232 serial port. The firmware includes independent heater driving in continuous mode, independent sampling for each sensor in the array and averaging of sensor measurements.

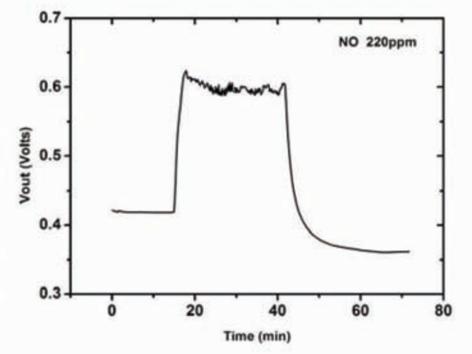


Fig. III.2.5: *Output of the ASIC with one commercial metal oxide sensor connected*

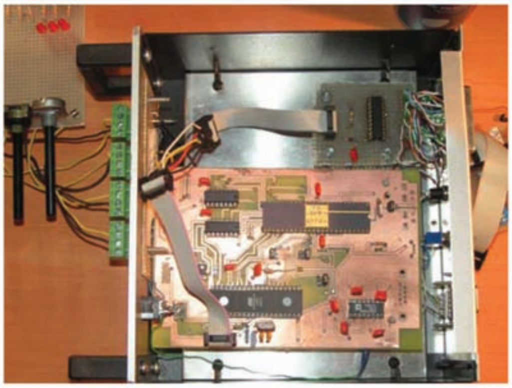


Fig. III.2.6: *ASIC and microcontroller PCB*

For more information please contact Dr. S. Chatzandroulis (e-mail: stavros@imel.demokritos.gr)

C. Polymer based chemical sensors

M.Kitsara, K.Manoli, D.Goustouridis, S.Chatzandroulis, I.Raptis

c_1 *Capacitive Interdigitated Electrode Chemical Sensors*

One of the simplest chemical sensing devices makes use of polymer coated InterDigitated Electrodes (IDEs) where the transduction mechanism relies on the permittivity changes and swelling of the coating polymer, to inflict a change in the capacitance between the two interdigital electrodes.

A single chip chemical sensor array based on IDEs has successfully been fabricated with conventional semiconductor processes (thermal oxidation, Al evaporation, optical lithography and wet etching). On those IDEs, polymers with photolithographic patterning processes have been applied as sensing layers. The use of a polymer as sensitive layer provides specific advantages compared to other chemical sensors. The major benefits include the ease of depositing the polymeric sensitive film to the desired geometric form and thickness due to use of lithographic methods. The whole fabrication, it is a batch process, compatible with microelectronic processes. In addition, polymers enable a good compromise between response time, selectivity and reversibility. The implementation of the whole sensor on Si wafers allows for future integration with CMOS signal conditioning circuits.

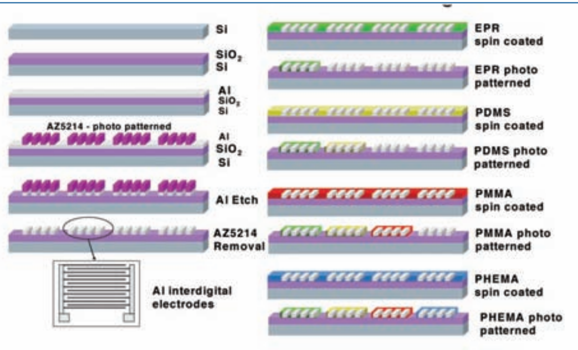


Fig. III.2.7: *Fabrication flowchart of the Inter Digitated Capacitor array*

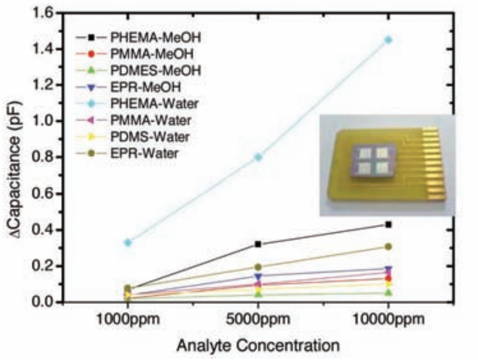
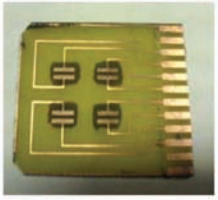


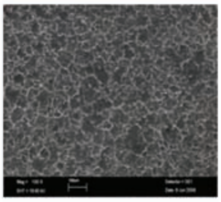
Fig. III.2.8: *a) Finished sensor array b) Response of the array to controlled concentrations (1000, 5000, 10000 ppm) of water and methanol vapors.5.*

c_2 Conductometric chemical sensors

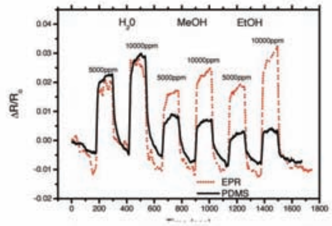
Conductometric chemical sensors based on polymer composite films, synthesized by adding conductive fillers to the polymer solutions and deposited between two predefined electrodes, are well established. Deposition of the sensitive composites is usually applied to sensor devices by solvent casting methods such as spin coating, spray coating and drop casting. These methods lack in pattern precision and repeatability. In order to overcome pertinent problems the application of conventional patterning methods for the fabrication of the conductive sensing array is proposed. In this work, we present the deposition of two conductive polymer composites (poly(dimethylsiloxane) /carbon black and epoxy polymer / carbon black on the same substrate. Each polymer composite is deposited onto two respective electrodes, effectively creating a conductive polymer chemical sensor pair. The two sensors performance is evaluated and considered as a first step towards the fabrication of a conductometric polymer composite array. Electrical vs. dimensional sensitivity issues and the significance of electrode configuration are considered.



Photograph of final sensor chip with four PDMS conductive polymer chemical sensors



SEM image of the patterned surface: PDMS



Response of both PDMS/CB and EPR/CB sensors to 5000 and 10000 ppm of water, methanol and ethanol vapors.

For more information please contact Dr. I. Raptis (e-mail: raptis@imel.demokritos.gr)

D. Capacitive Type Sensors

S. Chatzandroulis, D. Goustouridis, D. Tsoukalas, P. Normand

d_1 Pressure Sensors

In 2006 part of our activities on silicon micromachined capacitive pressure sensors were devoted to the development of advanced finite element models to approximate experimental behaviour. Pressure sensors typically consist of a thin silicon diaphragm which deflects when a pressure differential is exerted, and are usually modelled as having completely immovable edges and rigid unbendable substrates. The model we developed follows a realistic device approach by taking into account the whole sensor die body, including the substrate, the intermediate layers and the foundation onto which the sensor diaphragm stands. It also includes all nonidealities and stress components of the micromachined device.

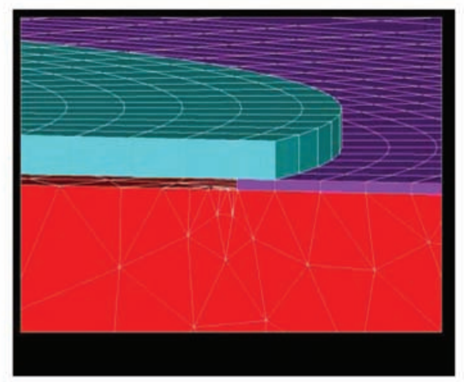


Fig. III.2.9: *Model detail of the sensor diaphragm rim lying on the oxide.*

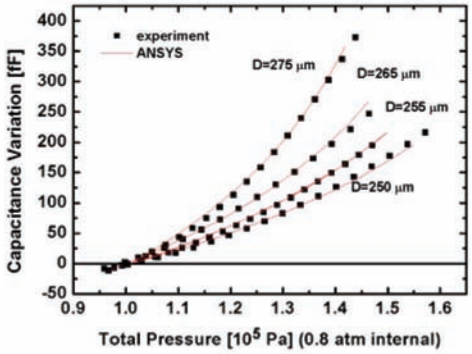


Fig. III.2.10: *Simulated and experimental sensor response after including residual stress for four sensor diaphragm diameters.*

d_2 Capacitive DNA Sensors Arrays

Unlabeled DNA detection has received a lot of attention in recent years as it simplifies sample preparation and testing procedures. To this end, we work towards exploiting surface stress changes and subsequent bending of microelectromechanical structures combined with capacitive detection. A first sensor employing capacitive detection and silicon micromachined membranes has been developed. The sensor accommodates in a single chip a capacitive DNA sensor array of 256 elements. Each sensor in the array consists of a single crystal silicon membrane that is covered with receptor DNA after surface functionalization and deflects upon exertion of surface stress hybridization. Membrane deflection is detected as a change in device capacitance. These activities are conducted within the frame of the European Project Micro2DNA.

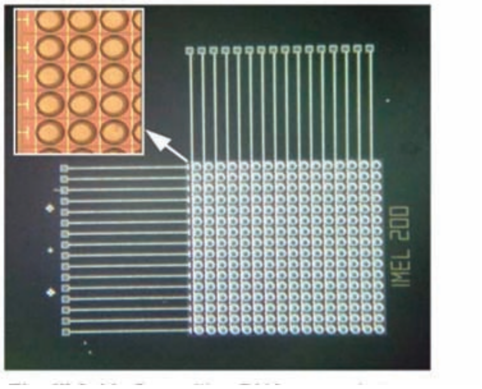


Fig. III.2.11: *Capacitive DNA array photo (top view) before Al deposition and functionalization*

For more information please contact Dr. P. Normand (e-mail: normand@imel.demokritos.gr)

E. Suspended Cantilevers for Electromagnetic Energy Harvesters

E. Makarona, C. Tsamis, S. Chatzandroulis, T. Speliotis, and D. Niarchos**

The proliferation of Micro-Electro-Mechanical Systems (MEMS) envisioned to be placed in remote locations, hazardous environments, or even within the human body raises the problem of power supply and data transmission. To solve this problem, sustainable power generation has to be achieved by harvesting ambient energy and converting into electrical energy. Our focus towards such a solution is the development of inertial electromagnetic micro-generators based on standard silicon technology.

The goal of this present work was the in-depth study of the engineering constraints and challenges one faces when integrating magnetic materials with silicon microstructures, as well as the determination of suitable fabrication conditions that would eventually allow the combination of optimal magnetic (fig III.2.12a) and mechanical (fig. III.2.12b) properties of the materials.FEM analysis of the structures was performed using Coventorware (fig. III.2.13a). Figure III.2.13b shows the simulated deflections as a function of the "effective" stresses that develop in the film. Estimation of the stresses that develop as a function of the growth conditions is obtained by comparison of the experimental and the simulation results. A process window has been determined in order to integrate magnetic material on suspended microcantilevers, with optimum magnetic and mechanical properties, suitable for electromagnetic microgenerators.

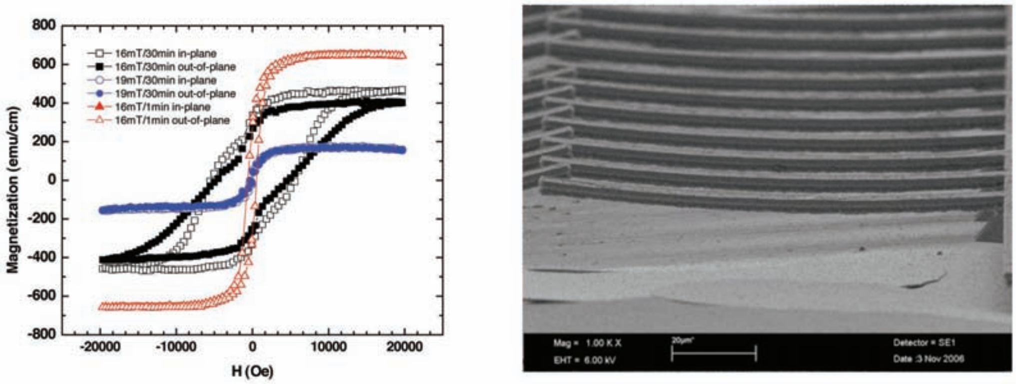


Fig. III.2.12: *(a) Magnetization loops for the in-plane (open) and out-of-plane (solid) magnetization as a function of the processing conditions, (b) Control of the stresses within the structure can be achieved through a compromise at the length of the annealing time and hence the magnitude of the magnetization of the magnetic film*

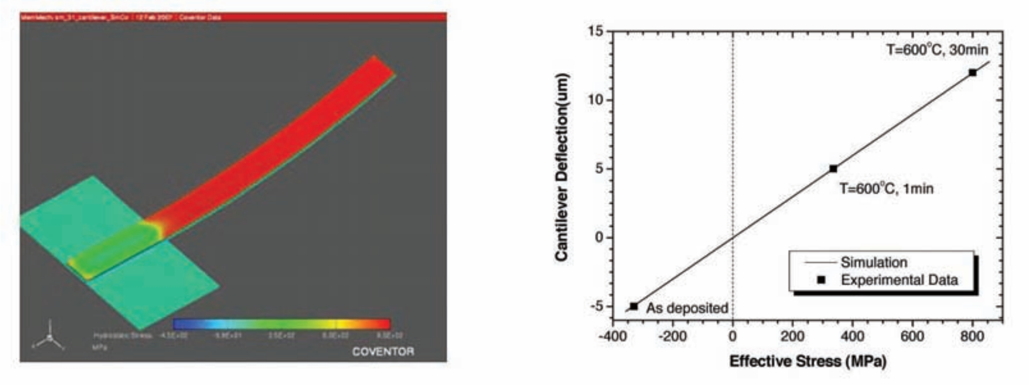


Fig. III.2.13: *(a) Stress distribution on the cantilevers as predicted from FEM analysis, (b) Estimation of the intrinsic stress from the comparison between simulated and experimental deflections.*

**This work is performed in collaboration with the Inst. of Material Science, NCSR "Demokritos"*

For more information please contact Dr. E. Makarona (e-mail: elmak@imel.demokritos.gr)

PROJECT OUTPUT in 2006

Publications in International Journals and Reviews

1. "A Lithographic Polymer Process Sequence for Chemical Sensing Arrays", M.Kitsara, D.Goustouridis, S.Chatzandroulis, K.Beltsios, I.Raptis, Microelectron. Eng. 83 1192(2006)
2. "Vapor sorption in thin supported polymer films studied by white light interferometry", K.Manoli, D.Goustouridis, S.Chatzandroulis, I.Raptis, E.S.Valamontes, M.Sanopoulou, Polymer 47 6117(2006)
3. "Capacitive Pressure Sensors And Switches Fabricated Using Strain Compensated SiGeB", S.Chatzandroulis, S.Koliopoulou, D.Goustouridis, D.Tsoukalas, Microelectron. Eng. 83, 1209 (2006).
4. "Capacitive Sensors", D.Tsoukalas, S.Chatzandroulis, D.Goustouridis, invited article in Wiley Encyclopedia of Medical Devices and Instrumentation, Second Edition, vol. 2, pp. 1-12 (2006).
5. "Alternative microhotplate design for low power sensor arrays", R. Triantafyllopoulou, S. Chatzandroulis, C. Tsamis and A. Tserepi, Microelectronics Engineering, Vol. 83, 1189 (2006)
6. "Integrated circuit interface for metal oxide chemical sensor arrays", P. Robogiannakis, S. Chatzandroulis and C. Tsamis, Sensors and Actuators A: Physical, Volume 132, Issue 1, Pages 252-257 (2006)

Publications in Conference Proceedings

Conference Presentations

1. "Single chip interdigitated electrode capacitive chemical sensor arrays", M.Kitsara, D.Goustouridis, S.Chatzandroulis, I.Raptis, R.Igreja, C.J.Dias, EuroSensors 2006, Sept. 2006, Goeteborg, Sweden (Poster)
2. "Fabrication of conductometric chemical sensors with a novel lithographic method", N.Andreadis, S.Chatzandroulis, D. Goustouridis, K.Beltsios, I.Raptis, MNE 2006 Micro & Nano Engineering 2006, September 2006, Barcelona, Spain (Poster)

3. "Patterning of PDMS/carbon black conductive polymer composite for chemical sensors fabrication", N.Andreadis, S.Chatzandroulis, D.Goustouridis, K.Beltsios, I.Raptis, Micro Process & Nanotechnology 2006 October 2006, Kanagawa, Japan (Poster)
4. "Impact Of Structural Parameters On The Performance Of Silicon Micromachined Capacitive Pressure Sensors", G. Bikakis, V. Tsouti, S. Chatzandroulis, D. Goustouridis, P. Normand, D. Tsoukalas, in Eurosensors XX in Göteborg, Sweden, September 17-20, 2006.
5. "SnO2 sensors integrated on porous Si microhotplates to detect NH3", M. C. Horrillo, I. Sayago, J.P. Adrados, J. Gutiérrez, R. Triantafyllopoulou, S. Chatzandroulis, C. Tsamis, Eurosensors XX, Goteborg, Sweden, September 17-20, 2006 (Oral)
6. "Pulsed mode operation of low power SnO2 sensors for improved gas selectivity", R. Triantafyllopoulou, C. Tsamis, S. Chatzandroulis, M. C. Horrillo, J. Gutiérrez, Micro- and Nano-Engineering, MNE 2006, 17-20 September 2006, Barcelona, Spain (Poster)
7. "Implementation of hard magnetic thin films on suspended cantilevers for electromagnetic energy harvesters", E. Makarona, T. Speliotis, A. Darsinou, C. Tsamis, S. Chatzandroulis and D. Niarchos, SPIE Conference on "Microtechnologies for the New Millenium 2005", 2-4 May 2007, Maspalomas, Spain (Accepted for Oral presentation)

M. Sc. theses

1. "Sequential polymer lithography for chemical sensor arrays", M. Kitsara, Chemistry Dept./Uni. Athens, December 2006, Supervisors: I. Raptis, K. Beltsios
2. "Design and optimization of silicon nitride micro-hotplates for chemical sensors", N. Tokpasidou, Dept. of Informatics/Univ of Athens (April 2006), Supervisor: C. Tsamis
3. "Micromachining techniques in Germanium substrates for sensors and nano-devices", A. Konstantopoulou, Dept. of Informatics/Univ of Athens (July 2006), Supervisor: C. Tsamis

Diploma theses

1. "Characterization and modeling of suspended microstructures for sensor applications", N. Andreadis, Materials Dept./Uni. Ioannina, September 2006, Supervisors: I. Raptis, K. Beltsios
2. "Fabrication and Characterization of Micromachined Chemical Sensors", J. Kokkinis, Materials Dept./Uni. of Ioannina, October 2006, Supervisor: C. Tsamis
3. "Fabrication and characterization of vibrational energy harvesters based on piezoelectric elements", P. Papandreou, Materials Dept./Uni. of Ioannina, October 2006, Supervisors: E. Makarona/ C. Tsamis

Patents

1. "A Method to Deposit Multitude Polymer Materials for Chemically Sensitive Arrays", I.Raptis, D.Goustouridis, S.Chatzandroulis, M.Kitsara (OBI 20060100040)
2. "Capacitive pressure-responsive devices and their fabrication", S. Chatzandroulis, D. Goustouridis, D. Tsoukalas, P. Normand, Israel Patent No 151277, Publication date: 01-08-2006.

PROJECT III.3: BIO-MICROSYSTEMS

Project Leader: K. Misiakos

Key Researchers: A. Tserepi, I. Raptis, E. Gogolides, P. Argitis, H. Contopanagos

Post-doctoral scientist: K. Kotsovos

Objectives:

- Development of bioanalytical lab-on-a-chip devices based on monolithic optoelectronic transducers (bioactivated optocouplers). Development of white light interferometric setup for label free monitoring of biomolecular reactions.

Funding:

- EU, IST, STREP, "NEMOSLAB", NanoEngineered Monolithic Optoelectronic transducers for highly Sensitive and LAbel-free Biosensing (coordinated by K. Misiakos start 1-1-2006, end 31-12-2008)

RESEARCH RESULTS

- Optocoupler fiber tapering to micron dimensions and improved efficiency silicon LEDs.
- SU-8 microchannel integration on optocoupler chips.
- One dimensional protein based photonic crystal simulations towards label free detection of protein binding.
- Label-free protein detection through white light reflection interferometry

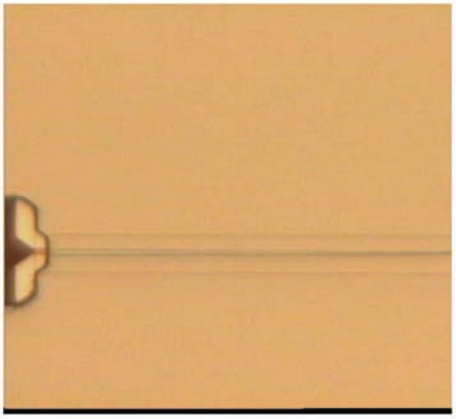


Fig.III.3.1: *Optocoupler fiber tapering from 4 to 1 micron.*

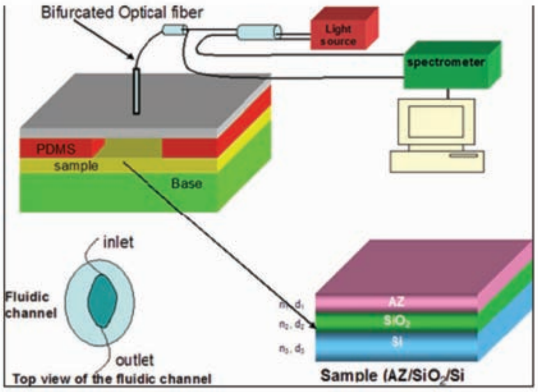


Fig.III.3.2: *White light interferometric set up. The protein layer built-up is determined from the red shift of the main interference peak.*

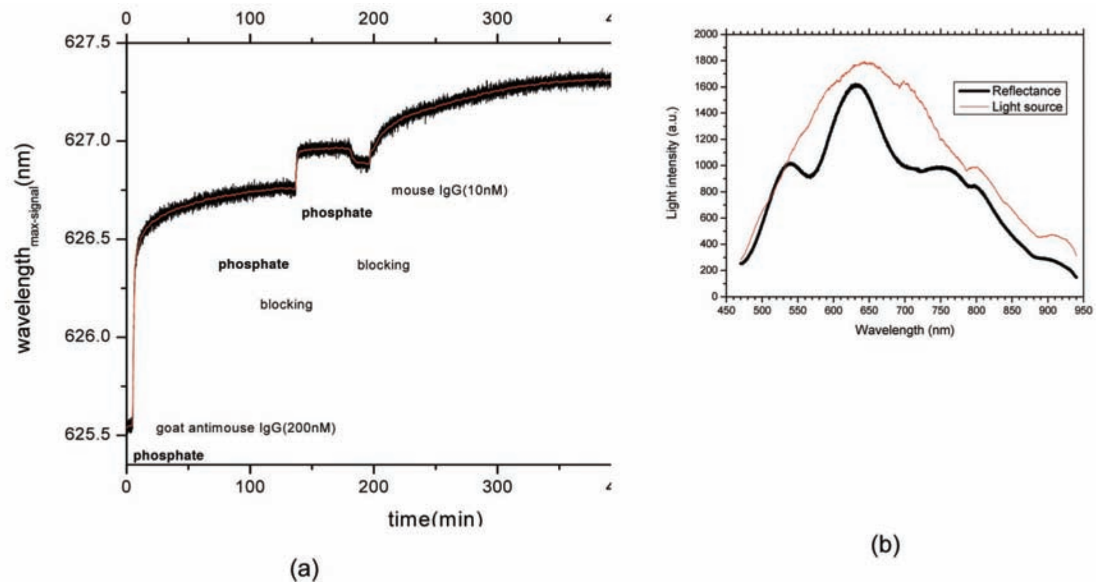


Fig. III.3.3: *Protein coating (goat antimouse IgG), blocking, and reaction steps (mouse IgG) monitored by the set-up in Figure2 (a). The observable is the main interference peak wavelength (b).*

Biomolecular interactions in real time by white light reflectance spectroscopy is demonstrated in Figure III.3.3. The experimental apparatus consists of a microfluidic channel for the supply of the biomolecular solutions placed above the sample on which the biomolecular interactions take place, and a reflection probe fiber to provide the probe beam on top of the sample through a glass window and guide the reflected beam to a spectrophotometer (Fig. III.3.2). The substrate used is a silicon wafer with a thick thermally grown silicon dioxide employed as the phase shift spacer to induce the interference pattern in the wavelength domain. Using this set-up it was possible to monitor in real time the protein film built-up during biomolecular coating, blocking and specific reaction to counterpart molecules. The biomolecular interactions were monitored as shifts of the wavelength of the main constructive interference peak and a formula was derived for translating these shifts into film thickness changes. The proposed methodology provides a simple, fast, low cost approach for a label free monitoring of biomolecular interactions. In future work, the study will be extended to other biomolecular interactions.

PROJECT OUTPUT in 2006

Publications in International Journals

1. "Label-free kinetic study of biomolecular interactions by white light reflectance spectroscopy", M. Zavali, P.S. Petrou, S.E. Kakabakos, M. Kitsara, I. Raptis, K. Beltsios and K. Misiakos, Micro & Nano Letters, Volume 1, Issue 2, p.94-98, 2006
2. "Monolithic silicon optoelectronic transducers and elastomeric fluidic modules for bio-spotting and bio-assay experiments",Misiakos, K., Petrou, P.S., Kakabakos, S.E., Vlahopoulou M.E., Tserepi A., Gogolides E., Ruf, H.H., Microelectron. Eng. 83, 1605-1608, 2006.
3. "Biochip-compatible packaging and micro-fluidics for a silicon opto-electronic biosensor", Ruf H.H., Knoll T., Misiakos K., Haupt R.B., Denninger M., Larsen L.B., Petrou P.S., Kakabakos S.E., Ehrentreich-Foerster E., Bier F.F. Microelectron. Eng. 83, 1677-1680, 2006.

Paper in International Conference Proceedings

1. "Monolithic silicon optoelectronic devices for protein and DNA detection", Misiakos, K., Petrou, P., Kakabakos, S.E., Vlachopoulou, M., Tserepi, A., Gogolides, E. (Invited Paper) Proceedings of SPIE - The International Society for Optical Engineering 6125, art. no. 61250W (2006)

International Conference Presentations

1. "Biomolecule friendly photolithographic process for sub-micron resolution patterning of proteins", Petrou P.S., Chatzichristidi M., Douvas A.M., Argitis P., Misiakos K., Kakabakos S.E., Biosensors 2006, Toronto Canada May 10-12, 2006. Abstract book P367.
2. "A bioanalytical microsystem based on a monolithic silicon optoelectronic transducer for real-time and label-free determination of multiple analytes", Petrou P.S., Mavrogiannopoulou E., Kakabakos S.E. Misiakos K., Biosensors 2006, Toronto Canada May 10-12, 2006. Abstract book O88.
3. "Photolithographic process based on high contrast acrylate photoresists for multi-protein patterning", Chatzichristidi M., Petrou P.S., Douvas A., Diakoumakos C.D., Raptis I., Misiakos K., Kakabakos S.E., Argitis P. MRS Fall Meeting 27 November-1 December 2006, Boston, MA, USA. Book of Abstracts p. 96. D15.15.
4. "Biofluid transport on hydrophobic plasma deposited fluorocarbon films", Bayiati P., Tserepi A., Petrou P.S., Kakabakos S. E., Misiakos K., Gogolides E., 32nd International Conference on Micro- and Nano-Engineering, MNE 2006, 17-20 September 2006, Barcelona, Spain. Book of abstracts p. 113, 4A – Micro- and Nano-systems for Biology 2.
5. "A novel process for irreversible bonding of PDMS and PMMaA substrates", M.E. Vlachopoulou, Tserepi A., Misiakos K., 32nd International Conference on Micro- and Nano-Engineering, MNE 2006, 17-20 September 2006, Barcelona, Spain. Book of abstracts p. 421 – Microsystems and their fabrication.
6. "Electroweting-based fluidic transport on hydrophobic fluorocarbon films deposited in plasma", Bayiati P., Tserepi A., Petrou P.S., Misiakos K., Kakabakos S. E., Gogolides E. 5th International Electrowetting Meeting, 31 May-2 June 2006, University of Rochester, New York, USA. Book of Abstracts

Greek Conference Presentations

1. "Label free kinetic study of biomolecular interactions by white light reflectance spectroscopy", Zavali M., Petrou P.S., Kakabakos S.E., Kitsara M., Raptis I., Beltsios K., Misiakos K., XXII Greek Conference on Solid State Physics and Material Science, September 24-27, 2006, Patra. Book of Abstract p.106.
2. "Simultaneous detection in real time of different BRCA1 gene mutations using a monolithic silicon optoelectronic transducer", Maurogiannopoulou E., Petrou P., Siafaka-Kapadai A., Christofodis I., Misiakos K., Κακαμπάκος Σ.Η. « 6th Greek Conference in Clinical Chemistry-Clinical Biochemistry, Athens, November 9-11 . Book of Abstracts p. 171.
3. "Label free kinetic study of biomolecular interactions by white light reflectance spectroscopy", Diploma Thesis at Institute of Microelectronics at NCSR Demokritos for Materials Science and Engineering department of University of Ioannina (October 2006)

Patent filing:

"Multianalyte biosensors based on monolithic optoelectronic transducers", PCT application, Filing No.: PCT/GR06/000069, Filing date: 27/12/2006, Priority: 20050100623/ 27-12-2005

PROJECT III.4: CIRCUITS & DEVICES FOR OPTOELECTRONIC INTERCONNECTIONS

Project Leader: G. Halkias (until July 2007)

Key Researchers: G. Halkias, S. G. Katsafouros, E.D. Kyriakis-Bitzaros

PhD Candidates: K. Minoglou

Research Associates: E. Grivas, P. Robogiannakis

Objectives:

The main objective of the project is the development of the technologies for future high-density and high-speed optoelectronic interconnections. In order to accomplish this objective the additional specific targets of optoelectronic device modeling and simulation, implementation of optoelectronic technology in spacecraft environment as well as packaging in terms of photonic link integration above CMOS integrated circuits have been identified.

Funding:

- EU- IST PICMOS, 2004-2007
- ESA- Multigigabit optical backplane for space applications, 2004-2006

RESEARCH RESULTS

A. Development of a model for simulating Vertical Cavity Surface Emitting Lasers (VCSELs) and driving circuit topologies

Motivated by the fact that the ability to model VCSEL optical behaviour is critical to the design and analysis of optoelectronic micro-systems, we developed a model, which combines the non-linear behaviour of the input parasitics with the intrinsic fundamental device carrier and photon rate equations. The complete model for the VCSEL is implemented by means of equivalent circuits for the fundamental device rate equations, the thermal effects, the non-linear gain and transparency number functions and the input parasitic elements. A systematic methodology for the model parameter extraction from dc and ac, electrical and optical measurements is developed. Model parameters are divided into three distinct groups and their determination is achieved by a three-step procedure. The first two steps of the procedure focus on the parameters of the VCSEL's input and use the dc I-L-V characteristics at different temperatures and the S_{11} parameters, while the third one is based on S_{21} parameter measurements at different bias currents and taking into account the already defined model parameters extracts the remaining ones which mainly refer to the optical output. The parameter extraction procedure is proved to be very fast while it preserves adequate accuracy. As shown in Fig.III.4.1 a and b, simulation results using the proposed model, is compared with the experimental measurements and present satisfactory agreement. Also, the transient response of the optical signal of a VCSEL is depicted in the form of eye diagrams at different frequencies using voltage pulse drivers in Fig. III.4.2 a and b.

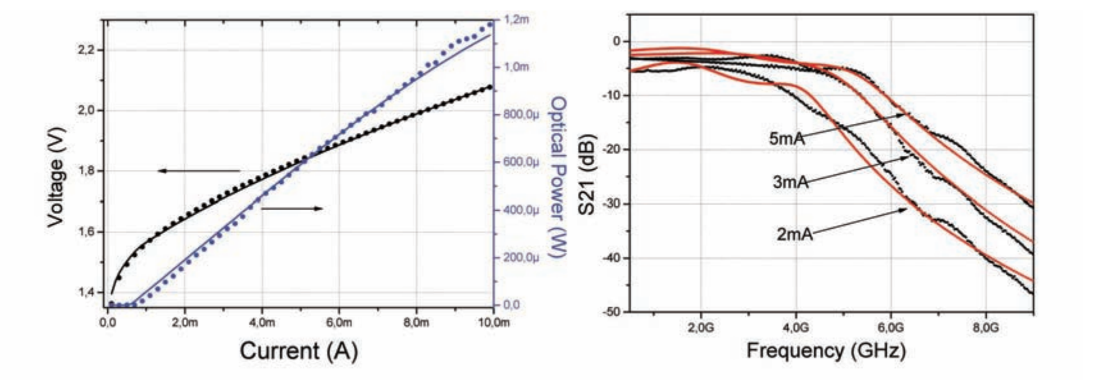
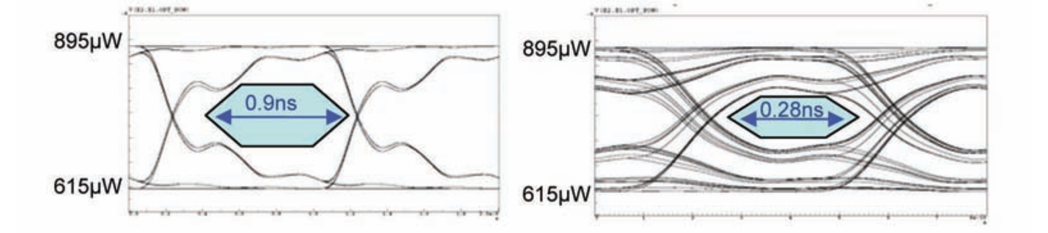


Fig. III.4.1: *(a) Measurements (dots) and simulations (continuous line)of DC I-V and I-L and (b) measured values (black line) and simulated (red line)* S_{21} *optical response at different bias currents*



(a) 1Gb/s

(b) 2.5 Gb/s

Fig. III.4.2: *Simulated eye diagrams with voltage pulse driving at different frequencies*

B. Multigigabit optical backplane for space applications

During the Extension phase of the project the most relevant protocols for the selected architecture were investigated and the appropriate recommendations were made. The different types of MAC protocols examined provide different characteristics in terms of network throughput, latency and bandwidth utilization. Moreover, the performance of each one is strongly related to the type of traffic it serves. As such, an effort to come-up with a type of protocol for use with the backplane proposed seems to be pointless. In contrast, several features of the protocols from these categories could be combined into a single protocol that provides different classes of services.

Random MAC: This class of protocols is the simplest one. There is no arbitration mechanism to allocate network resources and nodes comprising the network are in a continuous contention for resources. Packet collisions may happen at any time and when one occurs, packets have to be retransmitted. A back-off mechanism is often used to reduce the possibility of a collision between retransmitted packets. Random MAC protocols are very popular due to their simplicity that makes them a cost effective solution. Their theoretical performance is very poor, however, in practice they, surprisingly, seem to work. The most popular implementation of random protocols is the ALOHA protocol, while the Ethernet protocol was based on it.

Preallocation MAC: As its name implies, this class of protocols allocates network resources in advance of network utilization. The allocation is performed in a collision free manner, so that data is guaranteed to be transmitted error free. Point-to-point links is an example of a preallocation MAC protocol, where such a link is dedicated to the communication of two nodes. When multiple nodes share a common link (or part of it) Time Division Multiple Access (TDMA) may be employed. In such a scheme every time slot is preallocated to a pair of nodes. The set of every possible combination between pairs of nodes forms a cycle, which is repeated forever. These protocols offer great performance in terms of throughput at medium to high loads, but experience low network utilization at low traffic. The average packet delay is independent of the network load, but increases as the number of nodes increases. At a first glance it can be approximated as half the cycle time.

Reservation MAC: This class of protocols is the most sophisticated. It employs one or more control channels that are being used for resource reservation prior to data transmission. In that way data packet collisions are being prevented, while resources can be dynamically allocated to nodes leading to performance improvement at any possible type of traffic. Moreover, reservation protocols can support different arbitration mechanisms, so that they can offer a variety of Quality of Service (QoS). All these benefits provided by these protocols are in expense of an increased cost since the allocation of resources (wavelengths and slots) of the network should be calculated by a dedicated scheduler.

Random MAC protocols provide better performance in terms of latency and acceptable throughput when traffic is relatively low. They are suitable for computer networks, where data appear in short bursts and network resources remain unutilized most of the time. Pre-allocation MAC protocols offer guaranteed throughput under any type of traffic. Latency is strongly related to the number of nodes comprising the network. Finally, reservation MAC protocols offer better and more balanced performance, but at an increased cost and hardware complexity.

C. Heterogeneous integration of optical interconnects onto CMOS ICs

The ever decreasing transistor size has already begun to transfer the bottleneck of high-speed circuit performance from the active devices to the electrical interconnect. The employment of a photonic layer above CMOS integrated circuits (ICs) has been proposed as an alternative solution for the global interconnection regime. Photonic dies with fully integrated optical paths-sources and detectors coupled to waveguides are bonded onto a CMOS integrated circuit (IC) using a metallic bonding technique. The proposed approach utilizes a thin multilayer structure of the Au-20Sn eutectic alloy along with a thin starting layer of rare earth Gd and contains versatile structures for passive alignment. Its main advantage is the fact that it accomplishes mechanical bonding and electrical connectivity in a single step. The proposed approach resembles flip-chip approach, but the solder volume and size are considerably lower making it appropriate for high-density integration. Pattern uniformity, limited alloy spreading and contact resistance in the mΩ range across a 4-inch wafer has been verified. Fig. III.4.3 shows a patterned 4in wafer where convex structures are formed to match with the corresponding concave structures patterned on the dies. Fig. III.4.4 a and b present the patterns on wafer and on dies that are used for the metallic interconnect test measurements, while Fig. III.4.4c shows very good die-to-wafer achieved alignment. This project is executed in collaboration with IMEC, Belgium, ST, CEA, CNRS-FMNT, France, and TUE, Holland, in the framework of the European project PICMOS.

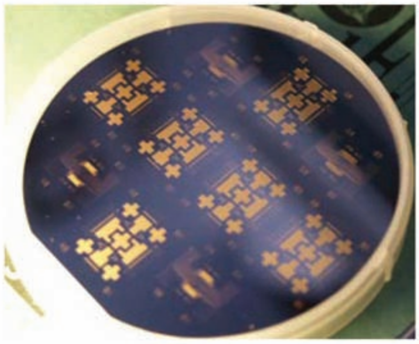


Fig. III.4.3: *Four-inch wafer with metallic lines and convex features (crosses) for alignment on it.*

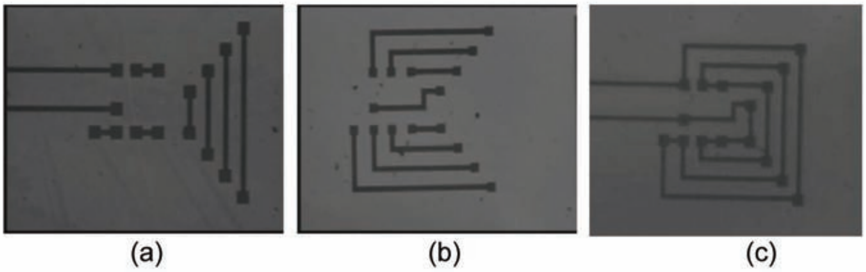


Fig.III.4. 4: *Appropriate patterns on the wafer (a), the dies (b), so that they can be used for the electrical tests after the bonding (c).*

PROJECT OUTPUT in 2006

Publications in Conference Proceedings

1. K.Minoglou, E.D. Kyriakis-Bitzaros, D. Syvridis, G. Halkias, "Input and Intrinsic Device Modeling of VCSELs", book of abstracts of IWCE 2006, pp.327-328 (presented in IWCE 2006, International Workshop on Computational Electronics, May 25-27, Vienna, Austria)
2. K.Minoglou,, E.D. Kyriakis-Bitzaros, D. Syvridis, A. Arapoyanni, G. Halkias, "VCSELs modeling and Simulation", proceedings of PRIME 2006, pp.201-204 (presented in PRIME 2006, June 12-15, Otranto, Italy)
3. E. Grivas, E.D. Kyriakis-Bitzaros, G. Halkias, S. Katsafouros, G. Morthier, P. Dumon, R. Baets, T. Farrell, N. Ryan, I. McKenzie, and E. Armadillo, "WDM Based Multigigabit Optical Backplane for On-Board Applications", Int. Conference on Space Optics, 27-30 June 2006, ESA/ESTEC, Nordwijk, The Netherlands
4. P. Robogiannakis, E. D. Kyriakis-Bitzaros, K. Minoglou, S. Katsafouros, A. Kostopoulos, G. Konstantinidis and G. Halkias, "Heterogeneous integration technique of optoelectronic dies to CMOS circuits via metallic bonding", ESTC 2006, 1st Electronics Systemintegration Technology Conference, Dresden, Germany, 5-7 September 2006
5. E.D. Kyriakis-Bitzaros, E. Grivas, G. Halkias, S. Katsafouros, P. Dumon, G. Morthier, R. Baets, T. Farell, N. Ryan, I. McKenzie, and E. Armadillo, "A WDM Optical Backplane with AWG Based Passive Routing", Photonics in Switching Conference, 16-18 Oct. 2006,Heraklion, Crete, Greece

Conference Presentations

1. "A WDM Optical Backplane with AWG Based Passive Routing", E.D. Kyriakis-Bitzaros, E. Grivas, G. Halkias, S. Katsafouros, P. Dumon, G. Morthier, R. Baets, T. Farell, N. Ryan, I. McKenzie, and E. Armadillo, Photonics in Switching Conference, 16-18 Oct. 2006,Heraklion, Crete, Greece.
2. "WDM Based Multigigabit Optical Backplane for On-Board Applications", E. Grivas, E.D. Kyriakis-Bitzaros, G. Halkias, S. Katsafouros, G. Morthier, P. Dumon, R. Baets, T. Farrell, N. Ryan, I. McKenzie, and E. Armadillo, Int. Conference on Space Optics, 27-30 June 2006, ESA/ESTEC, Nordwijk, The Netherlands
3. "Heterogeneous integration technique of optoelectronic dies to CMOS circuits via metallic bonding", P. Robogiannakis, E. D. Kyriakis-Bitzaros, K. Minoglou, S. Katsafouros, A. Kostopoulos, G. Konstantinidis and G. Halkias, ESTC 2006, 1st Electronics Systemintegration Technology Conference, Dresden, Germany, 5-7 September 2006.
4. "Input and Intrinsic Device Modeling of VCSELs", K.Minoglou, E.D. Kyriakis-Bitzaros, D. Syvridis, G. Halkias, book of abstracts of IWCE 2006, pp.327-328 (presented in IWCE 2006, International Workshop on Computational Electronics, May 25-27, Vienna, Austria).

PROJECT III.5: THIN FILM DEVICES for LARGE AREA ELECTRONICS

Project leader: D.N. Kouvatsos

Other collaborating researchers: D. Davazoglou, F.V. Farmakis

Ph.D. candidates: D.C. Moschou, G.P. Kontogiannopoulos, L. Michalas (University of Athens).

Post-doctoral: M. Exarchos (University of Athens).

Funding:

- PENED contract, project code 03ED550, 19/12/2005 – 18/12/2008.
- GSRT bilateral project Greece-Serbia, Polysilicon TFT reliability, 1/11/2004 – 31/10/2006.

Objectives:

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors fabricated in such films. Specifically, the targets are:

- Investigation of the influence of the polysilicon crystallization technique and film thickness on TFT performance, defect densities and degradation for ELA technology optimization.
- Evaluation of device parameter (a) hot carrier and (b) irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films.
- Investigation of effects of variations in TFT structure and fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Evaluation of bias stress-induced instabilities in solid phase crystallized (SPC) TFTs.

RESEARCH RESULTS

A. Characterization of ELA TFTs of varying technologies and structures

The characterization of TFTs made in sequentially laterally solidified (SLS) ELA polysilicon films has proceeded with the investigation of both different polysilicon crystallization technologies and different device structures. Advanced variations of the SLS ELA technique have been investigated and compared to the original directional technique. Furthermore, the performance parameters and characteristics of TFTs having top gate, bottom gate and double gate structures have been extracted and useful information for technology development has been obtained.

TFTs in "directional" SLS ELA films have very elongated grains along a preferred direction. Advanced variations of the SLS ELA technique, utilizing laser exposure through masks with many parallel slits, have been introduced to increase throughput, resulting in so-called 2-shot, 2^N-shot and MxN polysilicon films which have engineered rectangular grain shapes; a preferred direction still exists along the larger grain dimension but vertical boundaries also exist. TFTs in these advanced films have been characterized; the intragrain material quality was found to be higher for 2^N-shot devices, as evidenced by a lower grain boundary trap density, extracted following a Levinson analysis. The average device parameters, for top gate TFTs with various polysilicon film crystallization technologies, are summarized in the following table:

Crystallization technology	Field Effect Mobility, μ (cm²/V·sec)	Threshold Voltage, V_{th} (V)	Subthreshold Slope, ***S*** (mV/dec)	Grain Boundary Trap Density, N_t (cm^{-2})
directional	320	-1.1	130	4.9×10^{11}
2-shot	282	-1.8	390	6.5×10^{11}
2^N-shot	188	0.2	160	3.8×10^{11}
M×N	289	-0.2	170	3.4×10^{11}

In polysilicon TFTs localized traps near the drain augment free carrier generation-recombination rates, giving rise to parasitic bipolar effects through the back-interface area that enhance the drain current. In directional TFTs no boundaries intersect the current; only a low density of recombination centers exists. The parasitic bipolar action by transport of generated minority carriers is thus expected to be enhanced, yielding an additional excess IDS. This is confirmed in Figure III.5.1, which shows the output I_{DS}-V_{DS} characteristics for TFTs in 2^N-shot, 2-shot or directional polysilicon films; directional TFTs exhibit a higher excess drain current. It is thus determined that the susceptibility to drain current avalanche effects is lower for TFTs in advanced 2^N-shot polysilicon films.

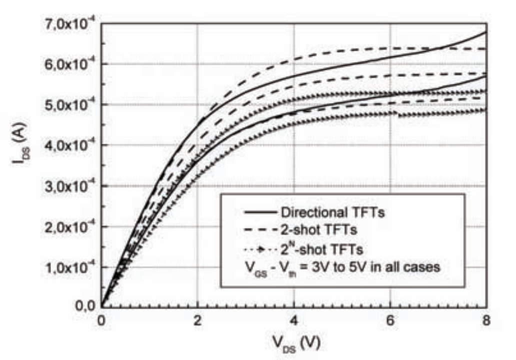


Fig. III.5.1: *Output characteristics of TFTs in 2^N-shot, 2-shot or directional polysilicon films.*

ELA TFTs oriented along a non-preferred direction are also under investigation, typically yielding significantly lower carrier mobilities and higher trap state densities. Moreover, in addition to advances in polysilicon crystallization technology, variations in TFT achitecture also offer enhanced performance characteristics and flexibility for the design of TFT-based circuits. TFTs having bottom gate (BG) and double gate (DG) structure have been investigated, as well as top gate (TG) ones. Double gate TFTs (top and bottom gate lengths L_t, L_b) offer the possibility of operation either from the top or from the bottom gate, with the opposing gate held at a given bias. As seen in Figure III.5.2, for both operation modes the transfer characteristics exhibit higher drain current for smaller L_b. This indicates that the presence of the back gate, while beneficial in terms of threshold voltage control, avalanche suppression or other electrical aspects, allowing more flexibility in circuit design, has to be optimized to avoid deleterious effects on the DG TFT characteristics due to inferior bottom interface quality.

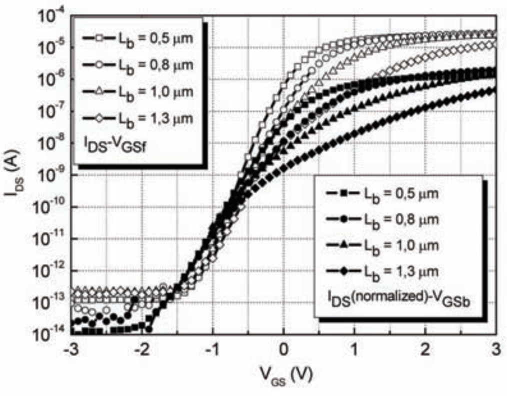


Fig. III.5.2: *DG TFT I_{DS}-V_{GSf} (for V_{GSb} = 0 V) and I_{DS}-V_{GSb} (for V_{GSf} = 0 V) characteristics, at V_{DS} = 0.1 V.*

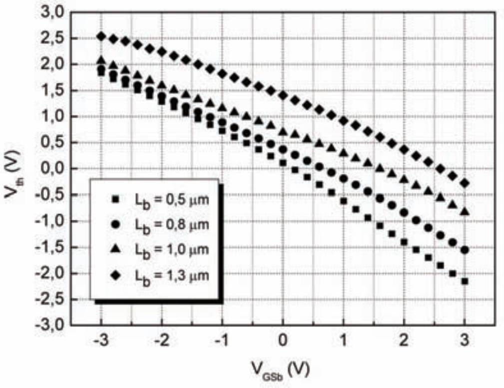


Fig. III.5.3: *V_{th} of DG TFTs for front operation against back gate bias, for TFTs with L_f = 1.6 µm and L_b ranging from 0.5 µm to 1.3 µm.*

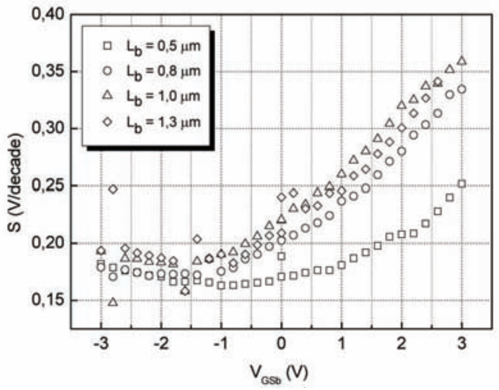


Fig. III.5.4: *Swing of DG TFTs for front operation against gate bias, for TFTs with L_f = 1.6 µm and L_b ranging from 0.5 µm to 1.3 µm.*

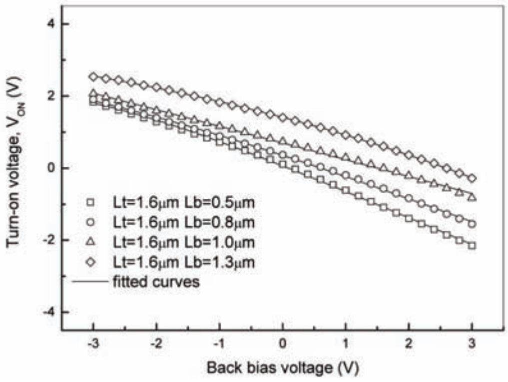


Fig. III.5.5: *V_{th} data and model fit against back gate bias voltage for asymmetric double gate TFTs (W = 8 µm) with various L_t / L_b ratios.*

The continuous V_{th} shift (Fig. III.5.3), without a plateau, indicates full depletion of the polysilicon films. For increasingly negative values of V_{GSb}, the values of V_{th} and, even more, of ***S*** (Fig. III.5.4) tend to cluster together. This is ascribed to the fact that the top operation of the DG TFT, due to the asymmetry in the values of L_f and L_b, involves series double gate and top gate TFTs. As the bottom channel contribution is reduced and eventually cut off, the drain current flows solely from the top channel and the ***S*** and V_{th} values, which mostly depend on the interface quality, settle towards those of a top gate transistor, even in the double gate area. An effort to model Vth for an asymmetric DG TFT is in progress, with preliminary results predicting its dependence on Lb/Lt (Fig. III.5.5).

A process flow for TFTs on oxidized silicon substrates has been developed and the first devices have been fabricated at IMEL, either with SLS ELA crystallization at Sharp or furnace anneal at IMEL. Preliminary results indicate good quality devices. Process variations, like novel gate dielectrics, will be introduced in TFTs still in the fabrication process at IMEL. This will allow the investigation of the effects of these variations on SLS ELA TFT performance, prior to their being tested by the industry.

B. Hot carrier stress investigation

TFT degradation under hot carrier stress (HCS) was investigated for devices fabricated in advanced 2^N-shot polysilicon films, as compared to directional ones. Figure III.5.6 shows the V^{th} and ***S*** evolution with stress time for a HCS condition (V_{GS}, V_{DS}) = (5 V, 10 V), for TFTs in 2^6-shot polysilicon films or in directional ones, while in figure 7 the evolution of the maximum transconductance $G_{m,max}$ is shown. A "minimal" stress condition of (V_{GS}, V_{DS}) = (5 V, 5 V) is shown to only have a negligible effect on all parameters for TFTs in both kinds of films.

There is a V_{th} shift due to the application of the (5 V, 10 V) stress, which is positive for 2^6-shot polysilicon TFTs and negative for directional ones. TFT degradation depends on carrier injection in the oxide, on trapping at interface states and on trapping at states at polysilicon grain boundaries. In directional material the last mechanism, which would introduce positive V_{th} shift, is less probable, as no boundaries vertical to the current flow exist. It is thus observed that in directional TFTs, under this stress condition, where we have predominantly hole injection, V_{th} exhibits a negative shift. In 2^N-shot material all three mechanisms contribute and the slight positive Vth shift may be attributed to the influence of electron trapping in the vertical grain boundaries.

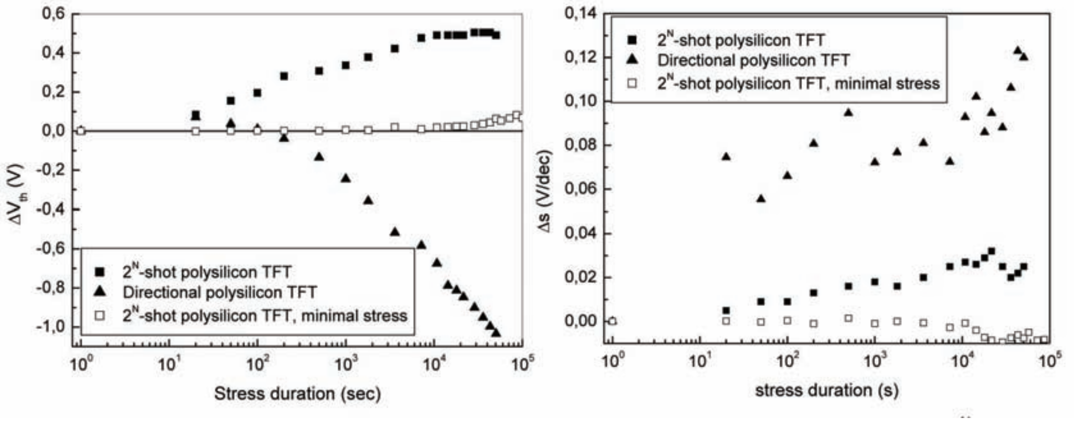


Fig. III.5.6: *Threshold voltage (left) and subthreshold swing (right) variation for SLS ELA TFTs in 2^N-shot or in directional polysilicon films, under a hot carrier stress (V_{GS}, V_{DS}) = (5 V, 10 V) or under a "minimal" stress of (5 V, 5 V).*

It is observed that the stress application results in a power-law time dependent Gm,max degradation for TFTs in both 2^6-shot and in directional polysilicon films, while the ***S*** degradation is present in both cases but is worse for directional TFTs. It is known that ***S*** depends mostly on deep trapping at the polysilicon / SiO_2 interface and / or on intra-grain state generation, while $G_{m,max}$ depends mostly on interface state generation and / or on grain boundary trap generation (tail-states). These data thus support the existence of two different HCS degradation mechanisms for 2^6-shot or directional polysilicon TFTs.

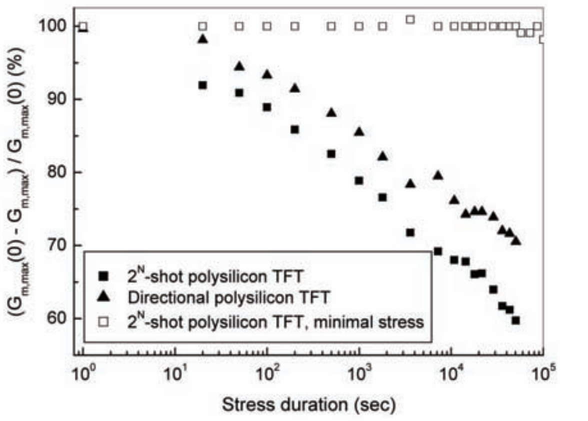


Fig. III.5.7: *Transconductance percentage variation for TFTs in 2^N-shot or in directional polysilicon films, under a hot carrier stress (V_{GS}, V_{DS}) = (5 V, 10 V) or under a "minimal" stress of (5 V, 5 V).*

C. Low temperature and transient current characterization

The inestigation of drain current transients, carried out in collaboration with the University of Athens, yields information critical for the assessment of the defectivity of polysilicon films obtained using various crystallization techniques. The obtained transients for SLS ELA TFTs are of the same order of magnitude at dark or under illumination and fall sharply at cryogenic temperatures, indicating polysilicon material of high crystalline quality with concentrations of generation-recombination centers much lower than those of standard SPC or ELA films. The device transient behavior temperature dependence, at dark or under illumination (Fig. III.5.8), suggests that the accountable mechanism cannot be attributed only to carrier trapping, but rather to a more complex mechanism involving carrier generation and recombination in the TFT body. It was determined that for ultra thin films the generation mechanism is different, possibly related to the proximity of the bottom interface, as evidenced by the data for 30 nm case not falling in line with those for 50 nm, 100 nm that show an exponential relationship between the generation lifetime and the activation energy (Fig. III.5.9). The dependence of thermally activated mechanisms on the film thickness suggests that the device operation is strongly related to the polycrystalline material properties.

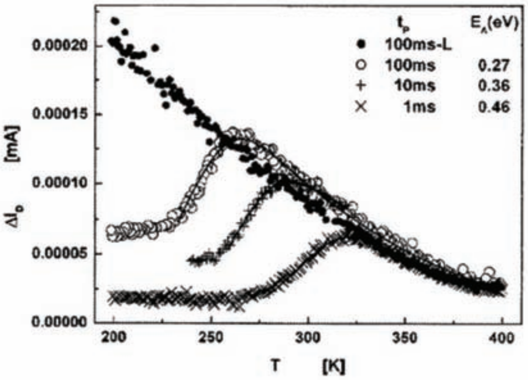


Fig. III.5.8: *Transient amplitude dependence of 50 nm TFTs on temperature for various off pulses; filled circles are for measurement under illumination.*

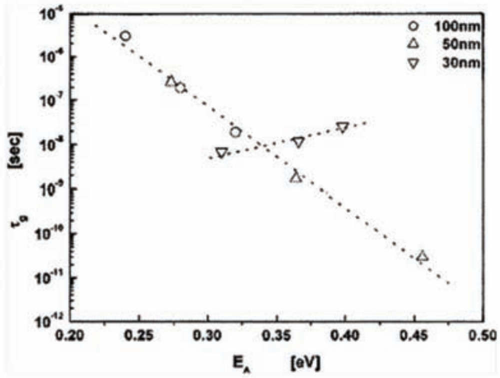


Fig. III.5.9: *Carrier generation lifetime against the activation energy for directional TFTs having active layer thickness of 30, 50 or 100 nm.*

D. Irradiation investigation

The degradation, under γ-irradiation, of the parameters of SLS ELA TFTs made in advanced "2-shot" polysilicon films has also been studied, in an investigation carried out in collaboration with the University of Nis, and compared with that for TFTs in directional films. It has been determined that 2-shot polysilicon TFTs are more resistant to γ-irradiation-induced degradation compared to directional ones. The characteristics of both 2-shot and directional ELA polysilicon TFTs for various irradiation doses, and anneals after the maximum dose, are shown in Figure III.5.10. The γ-irradiation of these TFTs results in positive oxide charge trapping, which induces negative V_{th} shifts. It is evident, from the larger negative shifts, that the irradiation-induced increases of the oxide trapped charges are smaller for TFTs fabricated in 2-shot polysilicon films. On the other hand, the subthreshold slope changes are similar, indicating similar interface degradation for TFTs of the two technologies.

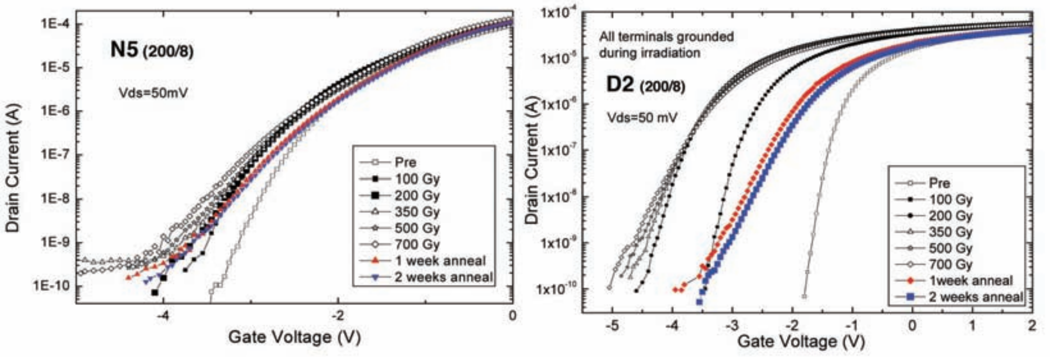


Fig. III.5.10: *Transfer characteristics* I_{DS}–V_{GS} *for 2-shot (left) and directional (right) SLS ELA polysilicon TFTs (W = 200 µm, L = 8 µm) for varying irradiation doses.*

E. Material characterization

The surface morphology and the grain structure of the polysilicon films depend on the crystallization technique. While directional films have a strongly preferential orientation, polysilicon films obtained with the advanced 2^N-shot technique exhibit engineered grain shapes with a high quality intragrain material, as shown, for comparison, in the SEM micrographs of Figure III.5.11. This difference in the material structure is reflected in TFT performance and reliability characteristics, as discussed in task 2. An investigation of the optical properties of advanced TFT gate dielectrics and of various SLS ELA polysilicon films, as a means for estimating their defectivity, is in progress.

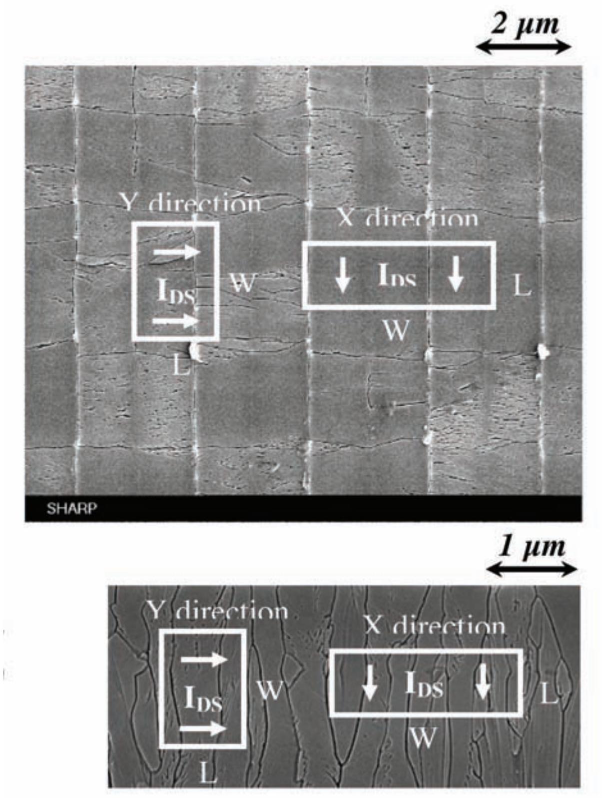


Fig. III.5.11: *SLS ELA polysilicon films obtained using 2^N-shot (top) or directional (bottom) techniques. Directions X (preferred) and Y are shown.*

PROJECT OUTPUT in 2006

Publications in International Journals and Reviews

1. Tsevas, S., M. Vasilopoulou, D.N. Kouvatsos, A. Speliotis and D. Niarchos, "Characteristics of MOS diodes using sputter-deposited tungsten or copper / tungsten films", Microelectronic Engineering, 83 (4-9), 1434, April-September 2006.
2. Exarchos, M.A., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "On the drain current overshoot transient in polycrystalline silicon transistors: The effect of hole generation mechanism", Journal of Applied Physics, 99 (2), 024511, January 2006.
3. Kouvatsos, D.N., A.T. Voutsas, L. Michalas, F. Farmakis and G.J. Papaioannou, "Device degradation behavior and polysilicon film morphology of TFTs fabricated using advanced excimer laser lateral solidification techniques", accepted to appear in Thin Solid Films.
4. Michalas, L., M. Exarchos, G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "An experimental study of the thermally activated processes in polycrystalline silicon thin film transistors", accepted to appear in Microelectronics Reliability.
5. Kouvatsos, D.N., F.V. Farmakis, D.C. Moschou, G.P. Kontogiannopoulos, G.J. Papaioannou and A.T. Voutsas, "Characterization of double gate TFTs fabricated in advanced SLS ELA polycrystalline silicon films", accepted to appear in Solid State Electronics.

Publications in Conference Proceedings

1. Farmakis, F.V., D.N. Kouvatsos, A.T. Voutsas, D.C. Moschou, G.P. Kontogiannopoulos and G.J.

Papaioannou, "Front and back channel properties of asymmetrical double-gate polysilicon TFTs", Thin Film Transistor Technologies VIII Symposium, Electrochemical Society Transactions 3 (8), 75, 2006.

2. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "The role of grain boundaries in the performance of poly-Si TFTs", Thin Film Transistor Technologies VIII Symposium, Electrochemical Society Transactions 3 (8), 87, 2006.
3. Michalas, L., M. Exarchos, G.J. Papaioannou, D. Kouvatsos and A. Voutsas, "Physics and electrical characterization of excimer laser crystallized polysilicon TFTs", Proceedings of the 25th International IEEE Conference on Microelectronics (MIEL 2006), Nis, Serbia & Montenegro, May 2006.

Conference Presentations

1. Farmakis, F.V., D.N. Kouvatsos, A.T. Voutsas, D.C. Moschou, G.P. Kontogiannopoulos and G.J. Papaioannou, "Front and back channel properties of asymmetrical double-gate polysilicon TFTs", The Electrochemical Society Extended Abstracts, vol. 2006-2, 2006 (210th Meeting of the Electrochemical Society, Cancun, Mexico, October 2006).
2. Michalas, L., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, "The role of grain boundaries in the performance of poly-Si TFTs", The Electrochemical Society Extended Abstracts, vol. 2006-2, 2006 (210th Meeting of the Electrochemical Society, Cancun, Mexico, October 2006).
3. Kouvatsos, D.N., A.T. Voutsas, L. Michalas and G.J. Papaioannou, "Device degradation behavior and polysilicon film morphology of TFTs fabricated using advanced excimer laser lateral solidification techniques", European Materials Research Society Spring 2006 Meeting, Symposium I: Thin Film Materials for Large Area Electronics, Nice, France, May 2006.

Conference Participation

Participation in the following conferences:

1. Spring 2006 European Materials Research Society Meeting, Nice, France, May 2006
2. 25th International IEEE Conference on Microelectronics (MIEL 2006), Nis, Serbia & Montenegro, May 2006
3. 210th Meeting of the Electrochemical Society, Cancun, Mexico, October 2006

Organization of Conferences, Workshops and Project Meetings

Reviewer – Member of the Technical Programme Subcommittee of the 25th International IEEE Conference on Microelectronics (MIEL 2006), Nis, Serbia & Montenegro, May 2006.

ANNEXES

ANNEX I

PERSONNEL

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11. Normand P.
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14. Tsamis C.
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2. Katsafouros S.

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1. Contopanagos H.

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7. Konstandoudis K. (Contract)
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10. Chatzandroulis S. (Contract)
11. Farmakis P. (Contract)

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5. Κοκονού M.
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10. Polymenakos S.
11. Vlachopoulou M.
12. Vourdas N.
13. Kitsara M.
14. Tatakis G.
15. Goupidenis P.
16. Malenou A.
17. Dimitrakis P. (Contract)
18. Gianetta V. (Contract)
19. Grivas E. (Contract)
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21. Kontogiannopoulos I. (Contract)
22. Kotsovos K. (Contract)
23. Salonidou A. (Contract)
24. Zacharatos F. (Contract)
25. Zoi A. (Contract)
26. Moschou D. (Contract)
27. Boulousis G. (Contract)
28. Triantafillopoulou R. (Contract)
29. Tsikrikas N. (Contract)
30. Drigiannakis I. (Contract)
31. Tsougenni A. (Contract)

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Makridis Z.
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Boukouras K. (Contract)
Georgiou C. (Contract)
Karmpadaki M. (Contract)
Linarakis E. (Contract)
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Kitsineli D. (Contract)
Kontakis K. (Contract)

ANNEX II

INFRASTRUCTURE AT IMEL

The infrastructure available at IMEL includes state-of-the art equipment and facilities for both micro and nanofabrication in a clean room area, and for design, modeling, characterization and testing of materials, devices, circuits and systems. A great part of the infrastructure has been funded through competitive projects at National and European level.
The clean room of a total area of 300m^2 has been fully upgraded in the year 2002.

The infrastructure available at IMEL includes the following:

I. Silicon processing laboratory in a clean room area of 300 m^2, equipped with the following:

- 4 laminar flow chemical benches
- 7 horizontal hot-wall furnace tubes
- 2 horizontal LPCVD tubes for nitride, oxide (TEOS), polysilicon
- 1 horizontal LPCVD tube for LTO
- Ion Implanter (EATON medium current, 200 KeV)
- Optical lithography systems (resolution down to 0,6 Ìm)
- Electron beam lithography system (resolution 50 nm)
- Reactive Ion Etcher
- Metallization equipment (thermal, e-gun evaporation, sputtering)
- Process inspection equipment

II. Processing equipment not in clean room:

- High Density Plasma Etcher
- Different thin film deposition systems
  - Sputtering
  - MOCVD

III. Characterization, Testing and Inspection Equipment

- *Electrical characterization equipment*
  - Karl Suss PA150 semi-automatic probe station
  - Karl Suss manual probe station
  - Micromanipulator probe station
  - RF probe station
  - HP measuring systems (4142B, 4084B, 8110A, 700i series, 4140B, 4284, 4192A, 34401, 16500A)
  - Keithley measuring equipment (230, 220, 617, 195A, 6517A)
  - Tektronix 224J Oscilloscope

- Oxford optistat Cryostat for temperatures in the range 4.2-320 K.
- Oxford DN cryostat for temperatures in the range 77-500 K

- *Optical characterization equipment*
  - Multiwavelength Spectroscopic Ellipsometer
  - FTIR system, model Tensor 27 of Bruker
  - Jobin Yvon spectrometer, wavelengths 300-1600 nm
  - Argon Laser
  - Oxford optistat Cryostat, 4.2-320 K
  - Emission spectroscopy set-up for electroluminescence measurements: USB-2000 spectrometer (Ocean Optics)
- *Morphology, structural characterization*
  - Leo 440 SEM
  - AFM (Veeco CP-II), STM (NT-MDT)
  - Stylus profilometer model XP-2 of Ambios Technology
- *Testing equipment*
  - Systems for testing of gas flow, gas, pressure, acceleration and humidity sensors.

IV. Modeling/Simulation Software

- *Process and device modeling software*
  - SILVACO Software (Athina, Atlas)
  - Suprem and Pisces
  - Floops and floods
  - Synopsys TCAD Tools
  - Software for MEMs modeling and simulation
  - Coventorware
  - FEM-LAB

V. VLSI Design Facilities

- *Hardware*
  - H-P 9000/ 700
  - SUN Ultra workstations
- *Software from schematic or VHDL to mask layout and verification*
  - Cadence
  - Mentor Graphics
  - Synopsis
  - Synopsis

New equipment purchased in 2006

- Scanning tunneling microscope STM/NT-MDT
- Atomic force microscope AFM/Veeco CPII
- SEM attachement for e-beam writing (Elphy/Raith)

- Automatic Dicing Saw, model DAD 321
- Equipment for optical measurements
  - Laser (at 325nm)
  - Detector (600-1600nm)
  - UV/VIS lamp with monochromator
- Vector Network Analyser (VNA-Anritsu system)
- RF probe station
- 12 ton heated press by Carver for microfluidics bonding and simple hot embossing experiments
- Fume Hood and Vacuum Oven (Lindberg Blue VO914A)
- Hewlett Packard 4278A 1 kHz/1 MHz Capacitance Meter
- Hewlett Packard 3488A - Switch Matrix
- Software for Process and Device modelling (Synopsys TCAD Tools)

ANNEX III

RESEARCH AND EDUCATION OUTPUT

LIST OF PUBLICATIONS IN REFEREED JOURNALS

1. "Photoluminescence lifetimes of Si quantum dots", Xanthi Zianni and A. G. Nassiopoulou, J. Appl. Phys. 100, 074312 (2006)
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25. "Surface Silylation of Epoxidized Polymers for Micromachining Applications", D. Kontziampasis, K. Beltsios, E. Tegou, E. Gogolides, 6th Panhellenic Polymer Conference, Patras 3-5 November 2006
26. "Stochastic modeling of roughness formation during etching of composite materials", E. Zakka, V. Constantoudis, E. Gogolides, XXII Panhellenic Conference of Solid State Physics and Material Science. Patras 24-27 September 2006
27. "Polydimethyl Siloxane Microfluidic chip for gas chromatographic separations", A. Malainou, ME Vlahopoulou, A. Tserepi, S. Chatzandroulis, XXII Panhellenic Conference of Solid State Physics and Material Science. Patras 24-27 September 2006
28. "Metallization using an epoxy resist and lift-off process for microsystem fabrication", D. Kontziampasis, E. Gogolides, XXII Panhellenic Conference of Solid State Physics and Material Science, Patras, 2006
29. M. Chatzichristidi, A. Douvas, P. Oikonomou, K. Misiakos, I. Raptis, C.D. Diakoumakos, P. Argitis, P.S. Petrou, S.E. Kakabakos, Photoresists for the fabrication of protein microarrays via multi-cycle lithography, Book of Abstracts, 6th Hellenic Conference on Polymers, Patras, 3-5.11.06, pp.118-9.
30. A. M. Douvas, K. G. Papadokostaki, K. Yannakopoulou, D. Niakoula, E. Gogolides, P. Argitis, Polyhedral-Oligomeric-Silsesquioxane (POSS) containing Resists for 193 nm Bilayer Lithography: The Effect of Partial Fluorination on the Lithographic Behaviour, Book of Abstracts, 6th Hellenic Conference on Polymers, Patras, 3-5 November 2006, p. 120
31. "Copper wire fabrication in macroporous Silicon templates", F. Zacharatos and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006

32. "Fabrication of SiO2 quantum dots on Si Substrate through porous aloumina mask", V. Gianneta, M. Kokonou and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006
33. "Porous anodic aloumina on Si as a template for Au nanowires fabrication", V. Gianneta and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006
34. "A novel microfabrication technology for plastic sensors formation", I. K. Tsougeni, G. Kaltsas, A. Petropoulos, P. Asimakopoulos, D. N. Pagonis and A. G. Nasiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006
35. "Integrated microflow sensor based on porous silicon technology", D. N. Pagonis,A. Petropoulos,G. Kaltsas and A. G. Nassiopoulou, XXII Panhellenic Conference of Solid State Physics and Materials Science, Patras, Greece, September 2006

INVITED TALKS

1. "Semiconductor quantum dots for nanoelectronic devices and on-chip integration", A. G. Nassiopoulou (Invited Talk), third Workshop on functional materials, FMA 2006, September 17-23 2006, Athens, Greece
2. "Micro-Nanoelectronics-Nanotechnology. The world of the infinitely small", A. G. Nassiopoulou (Invited Talk), 4th International Student Conference of the Balkan Physical Union, ISCBPU-4, Bodrum, 29/8-1/8/2006
3. "Lateral ordering of semiconductor nanocrystals within SiO2 for non-volatile memories and other nanoelectronic devices", A. G. Nassiopoulou (Invited Talk), NANOMAT-2006, Antalya, 21-23 June 2006
4. "Porous silicon for on-chip integration", A. G. Nassiopoulou (Tutorial), PSST-2006, Barcelona-Spain, 12-17 March 2006
5. "Silicon nanocrystal non-volatile memory devices", A. G. Nassiopoulou (Invited Talk), SINANO Workshop, Montreux, 22/9/2006
6. "Porous silicon for sensors and on-chip integration of RF components", A. G. Nassiopoulou (Invited Talk), 42th International Conference on Microelectronics, Devices and Materials and Workshop on MEMs, NEMs, September 13-15, 2006, Slovenia
7. "Lateral ordering of semiconductor nanocrystals within SiO2 for nanoelectronic devices", A. G. Nassiopoulou (Invited Talk), 3rd Workshop N&N, Thesssaloniki, 10-12 July 2006
8. "Light emission from silicon: Reality or dream?", A. G. Nassiopoulou (Invited Talk), 1st International Workshop on Transparent Conductive Oxides (IS-TCO 2006), Crete, 23-25 October, 2006
9. "Lateral ordering of semiconductor nanocrystals for memory applications", A. G. Nassiopoulou (Invited Talk), Workshop on Silicon Nanodevices Beyond CMOS: Emerging Nanodevices, RWTH Aachen, Germany, 7 – 8 November 2006
10. "Microelectronics-Nanotechnology: Present status and future trends", A. G. Nassiopoulou (Invited Lecture), University of Thessaloniki, 18/10/2006
11. "Quantum wires and dots, applications in Nanoelectronics and sensors", A. G. Nassiopoulou (Invited Lecture), University of Thessaloniki, 18/10/2006
12. "Monolithic silicon optoelectronic devices for protein and DNA detection", Misiakos, K., Petrou, P., Kakabakos, S.E., Vlachopoulou, M., Tserepi, A., Gogolides, E., SPIE Photonics West Conf: 21-26 January 2006, San Jose, California USA.

PhD THESES

1. "Nanocrystalline silicon for application in non-volatile memories", Doctoral thesis of A. Salonidou, Univerity of Athens 17/4/2006
2. "Arrays of semiconductor nanocrystals ordered in 2-D layers within SiO2 for application in memory devices", PhD thesis of A. Olzierski, Univerity of Athens 6/10/2006
3. "Nanoparticles as building blocks of electronic devices" P. Dimitrakis, National Technical University of Athens 20/12/2006
4. "Polymeric materials and processes for lithography on thin Films" D. Niakoula, Chemist, Chemistry Department of the University of Athens. Thesis Defence: November 2006
5. "Creation of Microelectronic Nanostructures and Nanodevices using Oxometallic compounds" D. Velesiotis, IT Department of the Univesrity of Athens, December 2006

DIPLOMA THESES

1. Master's Thesis: "Nanosciences and Nanotechnologies", G. Poulis, Defence: University of Thessaloniki, 18/10/ 2006
2. Master's Thesis: "Nanosciences and Nanotechnologies", T. Valsamidis, Defence: University of Thessaloniki, 18/10/2006
3. "Direct Study of biomolecular interactions by visible reflection spectroscopy", M. Zavali, University of Ioannina, Department of Materials Science and Technology (29/10/2006)
4. "Fabrication and evaluation of MOS devices for memory applications", G. Niarhos, National and Kapodistrian University of Athens, 9/2006
5. "Fabrication of nanostructures using P(S-bMMA) block copolymers as templates", K. Parisiadis, University of Ioannina 7/2006
6. "Development of and improvements on micromechanical nitride plates in chemical sensor applications", N. Tokpasidou, EPEAEK, IT Department, University of Athens, (May 2006)
7. "Micromechanical techniques used on Ge underlayers in sensor and nanodevice applications", A. Konstantopoulou, EPEAEK, IT Department, University of Athens, (July 2006)
8. "Fabrication and characterization of micromechanical gas sensors", I. Kokkinis, Department of Materials Science, University of Ioannina, October 2006
9. "Fabrication and characterization of piezoelectric elements for collecting energy from vibrations", P. Papandreou, Department of Materials Science, University of Ioannina, October 2006
10. Bachelor's Thesis "Conductivity sensors for volatile organic compound detection", N. Andreadis, University of Ioannina, Department of Materials Engineering, 09/2006
11. Master's Thesis "Study of absorption of a polymeric group (array) in the presence of organic vapors and its application on chemical sensors", M. Kitsara, University of Athens, Department of Chemistry M.Sc. programme on " Polymer Science and its applications", 11/2006
12. "Molecular transistors with organic crystals", M. Kalonakis, School of Applied Mathematics and Physics, iational Technical University of Athens, November 2006
13. "Electrical properties of molecular devices based on organic/inorganic composite materials", Ch. Livitsanos, School of Applied Mathematics and Physics, iational Technical University of Athens, November 2006

PATENTS

1. "Low power silicon thermal sensors and microfluidic devices based on the use of porous silicon sealed air cavity or microchannel technology", PCT patent, International publication, No W003/062134, Inter. Publ. date: 31/7/2003, Filing in USA, Japan Europe, China
2. "Multianalyte biosensors based on monolithic opotoelectronic transducers", Filing No.: PCT/GR06/000069, PCT patent, Filing date: 27/12/2006, Priority: 20050100623/ 27-12-2005, Misiakos K
3. "Capacitive pressure-responsive devices and their fabrication", Israel Patent No 151277, Publication date: 01-08-2006, S. Chatzandroulis, D. Goustouridis, D. Tsoukalas, P. Normand,
4. I.Raptis, D.Goustouridis, S.Chatzandroulis, M.Kitsara "A Method to Deposit Multitude Polymer Materials for Chemically Sensitive Arrays" (Application to greek patent office 01/2006)
5. P. Argitis, E. Gogolides, D. Niakoula, V. Vidali, E. Couladouros, R. Gautan, "Molecular resists based on polycarbocycle derivatives", PCT International Patent Application on September 19, 2006
6. P. Argitis, G. Pistolis, M. Vasilopoulou, Tuning the emitting color of single layer, patterned full color Organic Light Emitting Diodes, Greek Patent (OBI) appl. No 20060100359, 19 June 2006

PRODUCTS FOR POSSIBLE LICENSING OR OTHER DEVELOPMENT

1. Different sensor devices (pressure, acceleration, gas flow, gas composition measurements etc.)
2. Software for LER measurement and characterization from SEM images. Demo available on our web site http://www.imel.demokritos.gr/software.html
3. Software for nanolithography simulation and LER prediction based on Monte Carlo methods. Demo in Preparation
4. Software for topography evolution simulation during plasma processing. Demo to be released on our web site in spring 2007

ORGANIZATION OF CONFERENCES, SYMPOSIA, WORKSHOPS

1. *5th International Conference on Porous Semiconductors Science and Technology (PSST 2006), Sitges-Barcelona, 12-17.3.2006*. PSST 2006 was held in Sitges-Barcelona, Spain in the period 12-17 March 2006. Chairpersons of the Conference and Scientific Editors of the Proceedings were: *Leigh T. Canham (pSi-Medica, UK), Androula Nassiopoulou (IMEL, NCSR Demokritos, Greece) Vitali Parkhutik (Technical University of Valencia, Spain), Michael Sailor (University of California, USA)*. The Conference was attended by 250 people from 38 countries and 180 papers were presented in oral or poster sessions. The Conference Proceedings were published in a special issue of Physica Status Solidi. Available on line at www.interscience.com
2. *Symposium C within E-MRS IUMRS ICEM 2006, Nice 29/5 – 2/6/2006*. One of the 23 Symposia of the International Conference of E-MRS IUMRS and ICEM 2006 was organized by: *Androula Nassiopoulou, IMEL/NCSR Demokritos, Greece, Philippe Fauchet, University of Rochester, USA Laura Lechuga, IMN-CNM-CSIC, Spain*. The Symposium Proceedings were published in a special issue of Physica E. Available online at www.sciencedirect.com
3. *PICMOS STREP IST: 15-16 May*, 2006, Glyfada, Greece
4. *ESA- Multigigabit Optical Backplane Interconnections:* November 27, 2006, NCSR Demokritos, Athens
5. *Kick off meeting of NanoPlasma Project* April 6 2006
6. *Nano2life Summer School on Methods in Micro – Nanotechnology and Nanobiotechnology*. The

advanced Nano2life Summer school on Methods in Micro – Nanotechnology and Nanobiotechnology took place from June 26 to July 7, 2006 in the National Center of Scientific Research "Demokritos", Athens, Greece. Institutes of Microelectronics, Physical Chemistry, Material Science and Radioisotopes and Radiodiagnostic Products of Demokritos, as well as the Foundation for Biomedical Research of the Academy of Athens collaborated in the organization. 19 participants from several European institutes (16 from Nano2Life) followed the summer school. The educational background of the participants was very high. The school program including lectures (45 hours) and hands-on experiments (30 hours) covered three sections:

- *Section 1:* Principles of biochemistry, cell biology, physics and microelectronics.
- *Section 2:* Core Nanobiotechnology methods and practices
    - *Unit 2.1:* Micro and Nano-fabrication science and technology
    - *Unit 2.2:* Nanomaterials for bio-applications, Characterization, Imaging
    - *Unit 2.3:* Molecular and Cellular biology and Applications
- *Section 3:* Towards Integrated Nanobiotechnology systems

7. Summer School by NCSR Demokritos. IMEL, in collaboration with the other 7 institutes of NCSR "Demokritos", contributes every year to the organization of the annual General Summer School of orientation and information on recent developments in research and technology. In the last summer school held at 10-21 of July 2006 in "Demokritos", researchers of IMEL provided 11 lectures in fields of:
   - *Advanced Materials and Nanotechnology and*
   - *Informatics, Telecommunications, Microelectronics.*

   The lectures were supplemented by visits to the clean room and the rest of laboratories of IMEL. More than 200 graduate and undergraduate students attended the lectures of the last summer school.

SEMINARS – LECTURES AT IMEL

1. "Application of advanced scanning probe microscopy methods in investigations of micro- and nano-structures", Dr. Teodor Gotszalk, Wroclau University of Technology, Poland, 28 Sept. 2006
2. "Growth of semiconductor nanocrystals using very low energy ion beam synthesis", Dr E. Kapetanakis, October 3, 2006
3. "Organic electronics: a plastic future", Dr L. Palilis, October 3, 2006
4. "Growth and optical properties of III-Nitrides based nanostructures for optoelectronic applications", Dr. Georgios Halambalakis, 4 October 2006
5. "The investigation of the mass loading influence on electrical parameters of AT-cut GaPO4 resonators", Dr. Irina Mateescu, National Institute of Research and Development for the Physics of Material, Bucharest,Romania, 10 October 2006
6. "Microfluidic devices, where micromachining technology meets life sciences", October 26, 2006
7. "Fabrication technologies for micro, nanostructures and devices based on polymers", Dr I. Raptis, November 3, 2006
8. "Theoretical nanotechnology: Electrical, thermal and optical properties of materials in the nanoscale", Dr N. Papanikolaou, 17 November 2006