INSTITUTE OF MICROELECTRONICS (IMEL)
NCSR "DEMOKRITOS"

IMEL - NCSR "DEMOKRITOS"

CENTER OF EXCELLENCE IN MICRO, NANOTECHNOLOGIES AND MICROSYSTEMS

Annual Report

2005

Aghia Paraskevi, Athens
GREECE
www.imel.demokritos.gr

PREFACE

IMEL (Institute of Microelectronics) has been established in the year 1986 as one of the eight Research Institutes of NCSR Demokritos (National Center for Scientific Research), a medium size, multidisciplinary Research Center under the General Secretarial for Research and Technology of the Ministry of Development.

Through 20 years of research and technology, IMEL has developed experience and expertise, as well as unique technological advantages, which place it among the main EU Research Institutes in the field of Silicon (Si) technologies. The strong advantages of IMEL are as follows:

- Its excellent staff, composed of a small number of experienced senior scientists, surrounded by a large number of young researchers, all fully devoted to their work
- Research facilities in silicon processing, micro and nanofabrication, characterization and testing, which are unique in Greece
- Important expertise and know-how, as well as important proprietary technologies, materials and devices. Its intellectual property (IP) portfolio continues to expand and opens important possibilities for collaboration with industry and transfer of know how

Research at IMEL is carried out at EU level through its participation in European research projects and networks of excellence, as well as in initiatives for providing advanced technology services at EU level. EU projects are across a number of specific priorities of the EU research Framework Programme, including mainly Information Society Technologies (IST), Nanotechnology, Materials and Production Processes (NMP), and Energy. IMEL's success in the above peer reviewed R&D funded programmes represents one of the strongest endorsements of IMEL's R&D competence and reflects the world-class standing of the Institute.

On national level the expertise and infrastructure of IMEL are unique in Greece, which makes its role for the country also unique in an effort to develop novel technologies, to transfer technology and know-how to the industry and to develop human potential, which constitutes the principal driving force for an industrial activity in high technology. Furthermore IMEL developed mechanisms to promote the field at national level through the establishment and coordination of thematic networks and scientific societies (MMN Network, Micro & Nano scientific society).

In this annual report, the research and education activities of IMEL are presented, together with the main achievements and results in the year 2005.

Dr A. G. Nassiopoulou
Director of IMEL
Member of the Board of Management
of NCSR Demokritos

For more information:

www.imel. Demokritos.gr
Tel. 00302106533781
e-mail Director: A.Nassiopoulou@imel.demokritos.gr

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MAIN RESEARCH RESULTS

IMEL at a glance

IMEL is one of the eight research Institutes of the multidisciplinary research center "NCSR Demokritos" in Aghia Paraskevi, a suburb situated 10 kilometers from the center of Athens.

Main Objectives of IMEL

The main objectives of IMEL are as follows:

- Long-term research into understanding phenomena, mastering processes and developing research tools.
- Development of fundamental knowledge
- Development of novel high added-value technology products and production processes
- Development of human potential by education and training activities
- Services in advanced technology
- Transfer of technology and know-how

The objectives of IMEL are in line with the government policy to promote excellence in research, high technology development and innovation at Research Institutes and to promote collaboration between academia and industry.

The objectives of IMEL are also in line with the European policy to maintain and increase EU competitiveness and sustainable development through design, development and dissemination of advanced technologies, including micro and nanotechnologies and systems. They are also in line with the EU objective to "achieve a critical mass of capacities needed to develop and exploit leading edge technologies for the knowledge- and intelligence-based products, services and manufacturing processes of the years to come".

Due to the existing infrastructure available at IMEL for silicon processing and micro-nanofabrication and the existing expertise and know-how developed, the role of the Institute is significant in contributing to increase the technological level of the country and to spread the knowledge through collaboration with Academia in research and education activities.

Research orientation

IMEL is mainly devoted to silicon technologies and their diverse applications in information processing, storage, transmission systems and telecommunications, environmental systems, medicine, healthcare, food industry etc.
Research Activities at IMEL are structured in 3 programmes, each of them being composed of smaller projects. A scientist is in charge of each research project, while a program representative is assigned for the management of each programme. The 3 programmes and the corresponding projects are as follows:

A. MICRO and NANOFABRICATION
    - Lithographic Polymers and Processes
    - Plasma Processing and Simulation for Micro and Nano Patterning
    - Front-end Processes for Micro and Nanodevices
    - Thin Films by Chemical Vapor Deposition (CVD)

B. NANOSTRUCTURES and NANOELECTRONIC DEVICES
    - Nanostructures for Nanoelectronics and Photonics
    - Silicon Nanocrystal Memories
    - Molecular Materials as Components of Electronic Devices

C. SENSORS and MEMS
    - Porous Silicon Technology for Sensors and on-chip Integration

- Mechanical & Chemical Sensors
- Bio-microsystems
- Thin Film Devices for Large Area Electronics
- Circuits and Devices for Optoelectronic Interconnections

The field of activities of IMEL is of paramount importance worldwide. Microelectronics has become a foremost driver of social and economic progress. The move to nano-scale devices, called nanoelectronics, further revolutionizes applications. The technologies developed at IMEL are necessary both in establishing a distinct and recognized role for the Institute at a European and international level and in supporting the national policies. More specifically:

Micro and nanofabrication

Research in this field is essential in supporting the development of microelectronics technology, where miniaturization plays a dominant role, pushing to the development of new materials and processes allowing the fabrication and proper functioning of the miniaturized devices.

Novel specific processes and schemes, and related materials, are also needed in the area of sensors and microsystems. Furthermore, the recent expansion of the broader field of Nanotechnology, referring not only to the fabrication of novel electronic and photonic devices but also to a large number of applications in areas such as biotechnology, medicine, health care, materials, environment, pushes strongly among others to the development of novel micro-nano fabrication routes suitable for these emerging applications. The expertise of IMEL researchers and its infrastructure provide the basis for the involvement in this emerging attractive field and significant results have been already demonstrated. The activity in this area enhances the impact of the Institute in the national research environment through collaboration with groups from other fields (e.g. biology, chemistry, medicine) that need support in order to launch and/or continue research effort to this exciting direction.

Nanostructures and nanoelectronic devices

The driving force in this program is the increasing need worldwide for technological innovations in Information and Communication Technologies (ICT) involving R&D which evolves more and more towards an atomic or molecular scale. The major objective in either pursuing Moore's law or finding alternative solutions is to further increase the performance of circuits within a given volume, to decrease power consumption for a given level of performance and to decrease cost.

Research at IMEL is carried out within EU projects and it aims at scientific and technological excellence and innovation, in collaboration with EU industrial partners. The importance of this activity for the country comes from the need to follow advanced technologies, to maintain the level of knowledge in this field, to support education, to spread the knowledge, to promote awareness of worldwide scientific and technological development and to promote applications.

Sensors and MEMs

The activity on sensors and MEMs is of strategic importance both for the country and for Europe. MEMs products have a number of distinguishing attributes that make them attractive for the advanced manufacturing industry of the coming century. These include:

- Suitability for low cost, high volume production
- Reduced size, weight and energy consumption
- High functionality
- Improved reliability and robustness
- Biocompatibility

This activity at IMEL started at the early nineties and the Institute develops novel technologies, devices and promotes technology transfer and patent licensing to the industry.

Education and Training at IMEL

Scientists in charge: A. Tserepi, N. Papanikolaou

Due to its unique infrastructure at a national level and the important expertise and know-how of its researchers, IMEL plays an important role in post-graduate education. It participates very actively in the following educational programmes, in collaboration with Greek universities, by providing special courses and laboratory training:

1. Post-graduate program in “Microelectronics” in collaboration with the University of Athens (for MSc and PhD degrees)
2. Post-graduate program in “Microsystems and Nanoelectronic devices” in collaboration with the National Technical University of Athens
3. Post-graduate program in “Nanosciences and Nanotechnologies” in collaboration with the University of Thessaloniki

Laboratories and Central Fabrication Facilities at IMEL

The facilities and equipment of IMEL are unique in Greece. They include a full silicon processing laboratory in a clean room area of 300 m^2 equipped with lithography (optical, e^- beam) and etching tools, thermal and chemical processing facilities, ion implantation, deposition of metals, dielectrics and poly- nanocrystalline silicon by physical and chemical processes (LPCVD, sputtering, e-gun and thermal evaporation), and process inspection equipment. Satellite laboratories include electrical and optical characterization, micromachining and packaging laboratory, resist development laboratory, electron microscopy (SEM, STM/AFM), sensor characterization and testing equipment.

The clean room area for thermal, chemical and reactive ion etching processes of the Institute has been fully upgraded to class 1000 in the year 2002.

A new building of the Institute is under construction, which will host the characterization laboratories.

Architect: **I. Papaconstantinou**

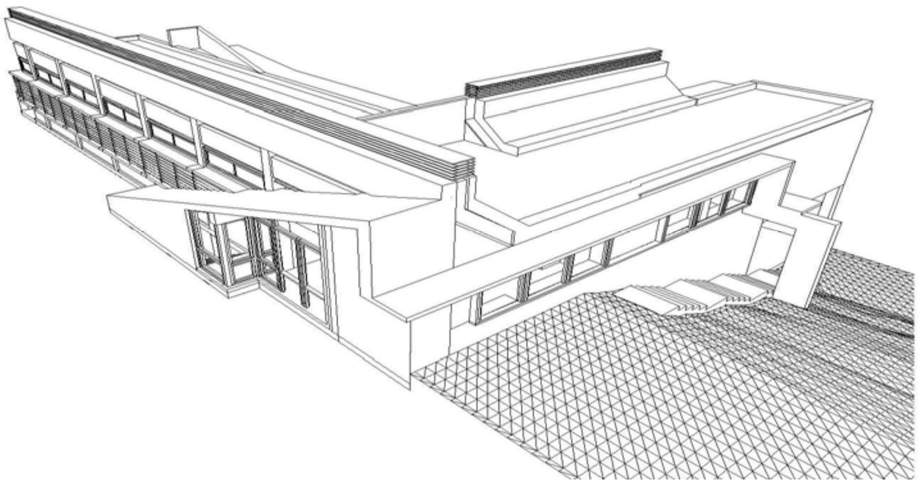


Fig. 01: *New Building of IMEL under construction*

Management

The management of the Institute is assured by its Director, who is elected by an International Scientific Committee for 5 years, assisted by a Deputy Director and an Institute Advisory Board, elected every 2 years by the Researchers. The Director represents the Institute in the Board of management of the Centre, and is responsible for the overall functioning of the Institute.

An external International Scientific Advisory Committee operates at IMEL from the year 2000, which discusses with the director and the scientific staff the Institute research priorities and policy.

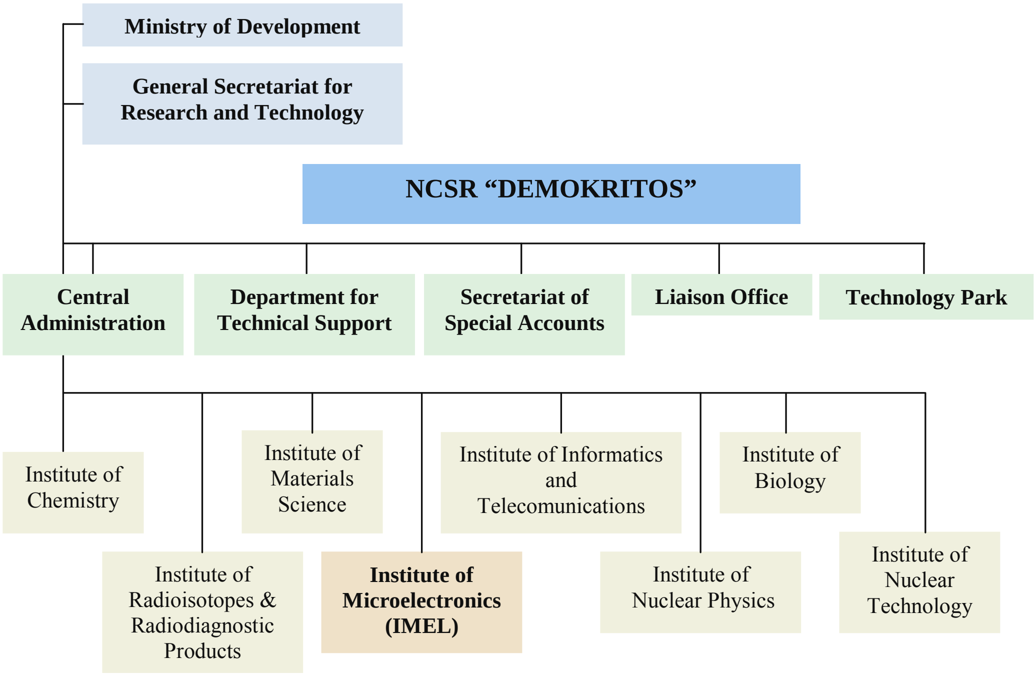
Personnel

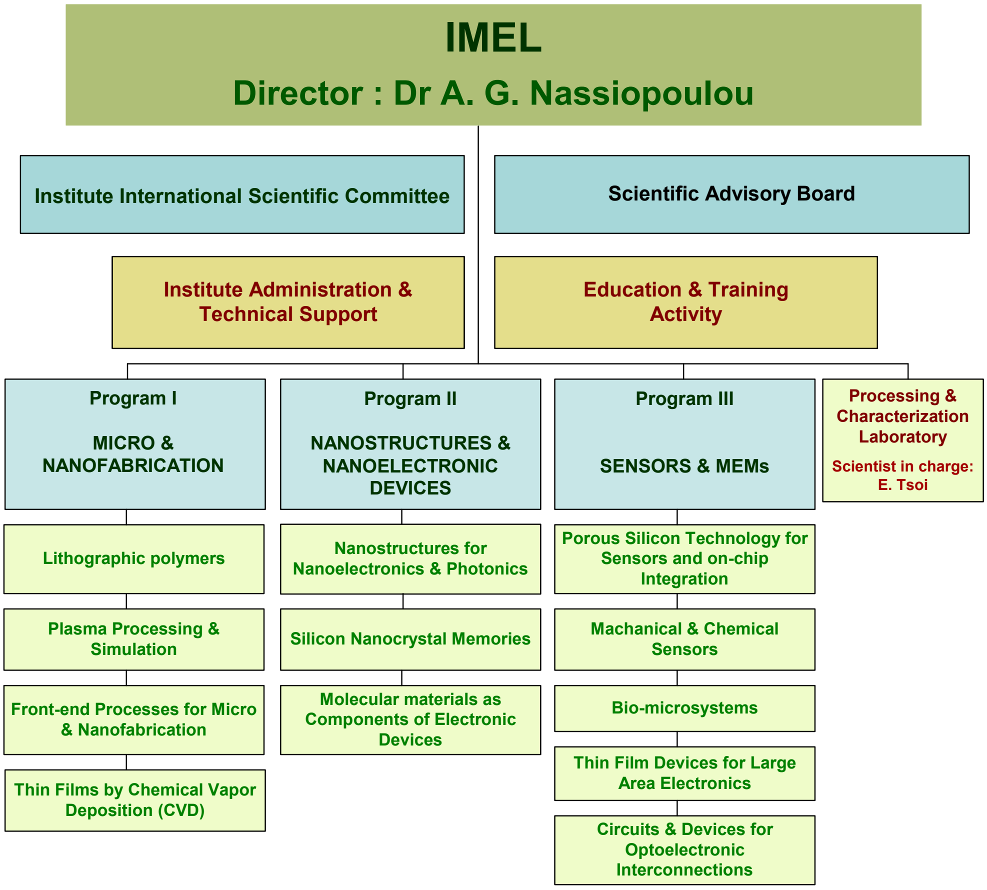
The personnel of IMEL is composed of 17 researchers, 1 research associate, 1 scientist on contract, 9 post-doctoral, 21 PhD students and 11 technicians and administrative personnel. The names of the personnel are given in annex I.

Fig. 02: *Scientific staff*

Fig. 03: *Personnel of IMEL*

ORGANIZATIONAL STRUCTURE of NCSR Demokritos & IMEL





PROGRAM I
MICRO and NANOFABRICATION

Programme representative: Dr P. Argitis

General

There are four scientific/technological areas at which the researchers of program I have focused their research activities, based on their scientific background and experience and the available infrastructure. These main research activities in the area of micro-nanotechnologies are the following:

a. Lithographic materials and related processes
b. Lithography and plasma processing
c. Front-End Processes and Simulation
d. Thin Films by Chemical Vapor Deposition

In overall the main objectives of program I can be summarized as follows:

- Development of advanced micro-nanofabrication processes and related materials following the roadmaps of Semiconductor Industry Association (SIA) on the miniaturization of CMOS circuits
- Development of novel processes and materials for the emerging broader field of micro–nano systems, with emphasis in bio-microsystems, microfluidics & photonics.
- Fundamental experimental, theoretical and simulation studies on micro-nanofabrication issues aiming at the understanding and optimization of processes, materials and characterization methodologies

IMEL has been established in the european and international level as having a good number of experienced researchers for conducting competent research at areas of significance according to the semiconductor industry roadmaps. The role of the Institute is well recognized in resist chemistry and processing, patterning schemes and pattern transfer processes, front end process simulation and CVD. Important international collaborations have been established with research centers, universities and leading companies in the field (INTEL, Photronics, ETEC). In the context of the above collaborations, lithographic materials and processes developed at IMEL are tested at the few sites available worldwide, in International Sematech (Austin USA), Sandia Labs (California USA), IMEC (Belgium), and ST Crolles (France). In addition, the more academic character of the Insitute compared to other silicon microelctronics institutes in Europe, allows a good involvement in the emerging field of microsystems and especially the one of Bionanotechnology. IMEL participates in the network of excellence Nano2Life, where it plays a leading role in the organization of an annual international summer school on nanobiotechnology hosted at NCSR Demokritos.

PROJECT I.1: LITHOGRAPHIC MATERIALS

Project leader: Dr P. Argitis
Key Researchers: Dr P. Argitis, Dr I. Raptis
Post-doctoral Researchers: Dr A. Douvas, Dr M. Vasilopoulou, Dr M. Chatzichristidi
Ph.D. candidates : D. Niakoula
Collaborating researchers from other projects: Dr E. Gogolides, Dr K. Misiakos

Funding

- EU IST-STREP SOARING, Contract N^o 35254, 1/3/2002-28/2/2005
- EU IST IP More Moore, Contract N^o 507754, 1/1/2004-31/12/2006
- EU NMP NoE Nano2Life, Contract N^o 500057, 1/2/2004-31/1/2008
- EU NMP STREP Microprotein, G5RD-CT-00744, 1/5/2002-31/10/2005
- Contract with the company INTEL- MoleEUV, 1/5/2003-30/4/2006
- GSRT bilateral project Greece-Poland, Polymeric films, 29/6/2004-26/6/2006
- GSRT bilateral project Greece-Hungary, Resist polymers (HARM.PB), 1/1/2005-31/12/2006

Research orientation:

- *Development of Resists for next generation lithography*

  Development of resists with potential for sub 45 nm patterning: "molecular" resists, self-organized systems, exploration of resist resolution limits
- *Materials research for fabrication of new devices and microsystems*

  Materials for novel radiation-assisted patterning processes such as flash nanoimprint, photochemically induced tuning of emission properties, microchannel formation

  Resists capable for patterning biological systems, and other sensitive materials under specified processing conditions.
- *Understanding Polymer Patterning Processes - Fundamental Physicochemical and Process Studies*

  Priority in understanding the physicochemical phenomena encountered in ultra thin polymeric films and interfaces, and in self-assembling-based patterning processes.

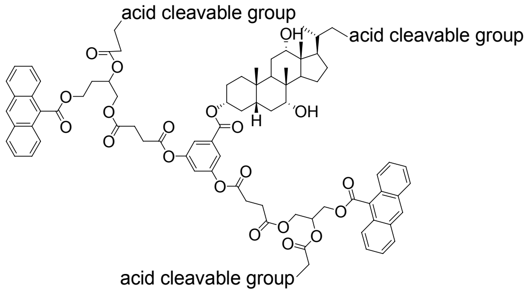
Main results in 2005

The main results obtained in 2005 within the different tasks of the project are given below.

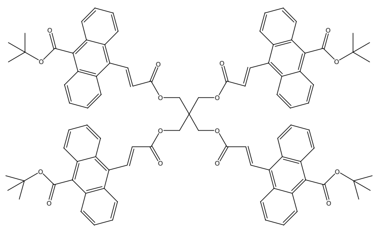
Task 1 Development of Resists for next generation lithography

New molecular resist materials based on polycarbocycle derivatives for EUV lithograhy

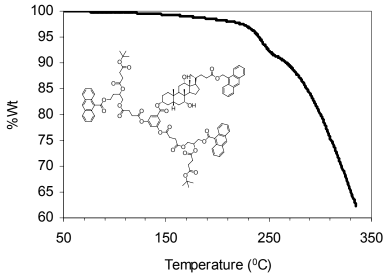
A new resist platform has been introduced by our group, based on the design and synthesis of new functionalized polycarbocycle molecules, which are used as the main components of resist materials. The synthesis work is carried out at the Inst. of Physical Chemistry (Prof. E. Couladouros). Resist formulations were developed at IMEL and evaluated under EUV (13 nm) exposure at International Sematech (Albany, NY, USA) and EPPRA (Paris, France). The obtained results proved that the proposed platform can give materials (molecular glasses) with sub 45 nm resolution capabilities, under the processing conditions preferred by the semiconductor industry (positive imaging with 0.26 N aqueous tertramethyl ammonium hydroxide developer). A patent was applied for while results were presented in EUVL workshop and MNE conference (invited presentations) and in Sematech 4th EUVL conference. Funding for this research effort has been obtained by INTEL and European projects “Soaring” (2002-2005) and “More Moore” (2006 -). Characteristic results are shown. Material and process optimization is under way to satisfy at the same time high resolution, LER minimization and sub 10 mJ/cm^2 sensitivity requirements.

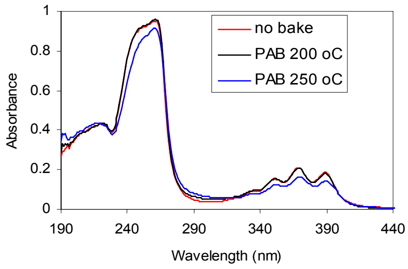


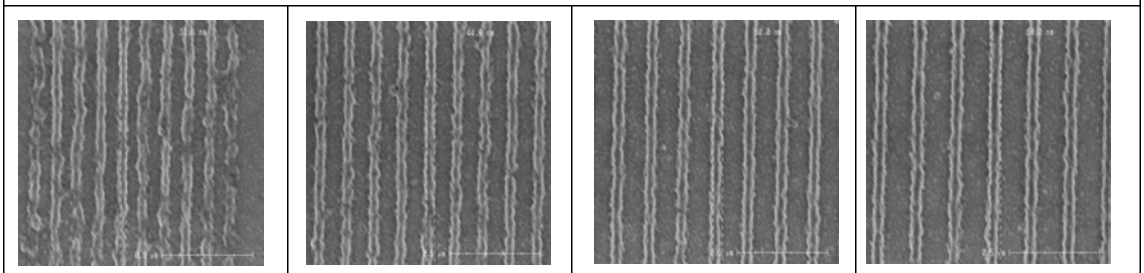
M17



M21







20 nm | 25 nm | 30 nm | 35 nm

Fig. I.1.1: *Characteristic novel polycarbocycle derivatives (M17, M21) used as main components of resist formulations (molecular glasses). Increased thermal stability is shown for the M17 based materials, and sub 40nm lithographic features obtained under EUV exposure for the M21-based resist formulations.*

Task 2 Materials research for fabrication of new devices and microsystems

Layer-by-layer UV micromachining methodology of epoxy resist embedded microchannels

A novel layer-by-layer fabrication approach for the manufacturing of long embedded microchannels has been developed. The methodology is based on the use of two epoxy based photoresist layers with different photo acid generator (PAG) concentration (fig. I.1.2a). The proposed UV based methodology is a very fast (wafer level) low cost process, making use of the conventional mask aligners and has no channel height limitations due to the low absorbance of epoxy polymer at 365nm. Using this methodology long, functional microchannels were demonstrated (fig. I.1.2b). The technology has been optimized through tuning of the epoxy molecular weight, PAG concentrations and processing conditions and a basic microfluidic application has been developed (fig. I.1.2c).

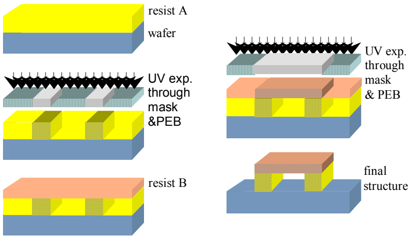


Fig. I.1.2a: *Schematic representation of the proposed methodology for the fabrication of embedded microchannels*

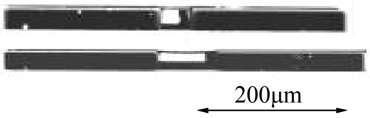


Fig. I.1.2b: *Cross-section images from SEM for 0.8mm long microchannels.*

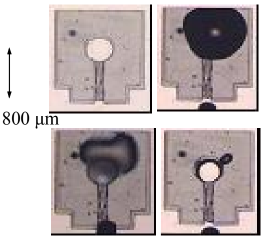


Fig. I.1.2c: *Water delivery steps through the microchannel.*

Patterning of magnetic structures

The fabrication and investigation of CoPt ordered structures is frontier research in the field of ultra high density magnetic recording media. However, despite the strong scientific and technological interest on tetragonal CoPt nanostructures. The aim of the work was the fabrication of magnetically hard 250 - 1000 nm $Co_{50}Pt_{50}$ ordered arrays, patterned by e-beam lithography by applying the lift off approach (fig. I.1.3a). For the lithographic process, 200nm PMMA resist (Mw 996K) was spin coated on cleaned Si wafers and prebaked at 160°C. The exposure was performed with a vector scan e-beam machine EBPG-3 at 50keV using a 500pA beam current at 100nm beam diameter. Development was performed in IPA-H_2O 7:3 for high resolution and sensitivity. The $Co_{50}Pt_{50}$ films, 50nm thick, were deposited by magnetron sputtering (IMS). After the growth, a lift-off step in acetone in ultrasonic bath was applied and dense structures with size down to 250nm were revealed (fig. I.1.3b, I.1.3c)

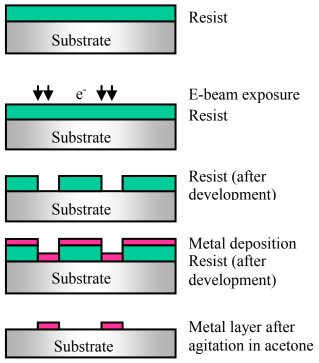


Fig. I.1.3a: *Lift-off process*

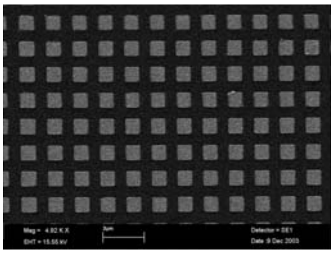


Fig. I.1.3b: *Top down SEM image of 500nm wide square arrays*

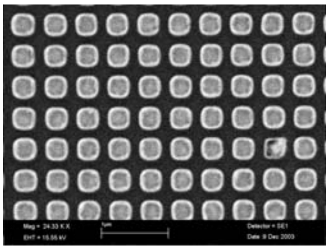
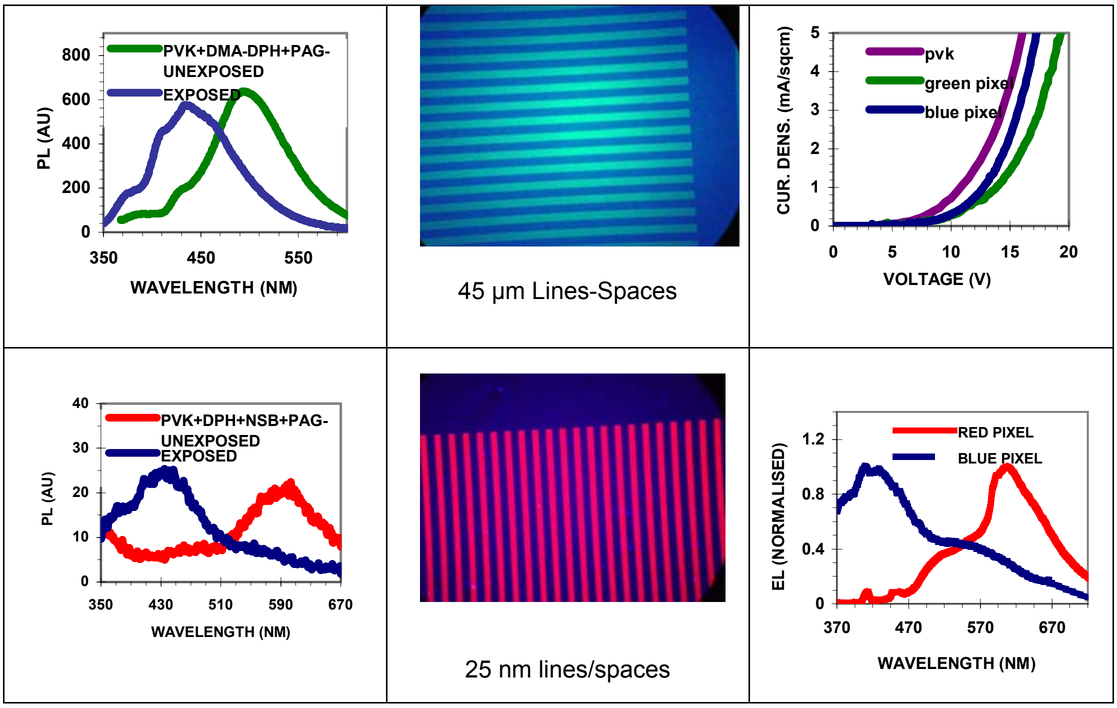


Fig. I.1.3c: *Top down SEM image of 250nm wide square arrays*

Novel patterning scheme for organic materials used in photonic applications

In the context of a new research activity, which started during the last years, aiming at the use of photochemically induced material transformations in photonic applications, results indicating the potential of the approach were obtained. In particular photochemically induced emission tuning for the definition of different colour emitting areas in conducting polymeric layers was demonstrated in order to define the three primary colour emitting pixels (red-green-blue) in the same polymeric layer, and thus to simplify full colour or white emitting light device fabrication. OLEDs (Organic Light Emitting Diodes) were fabricated and electroluminescence spectra showing similar shifts were recorded. The IV diode characteristics maintained their basic characteristics after the colour change (spectral shifts induced by photoacid generation) process. Representative results are shown.



45 μm Lines-Spaces

25 nm lines/spaces

Fig. I.1.4

Photopatternable POSS-based Polymeric Materials as low k Dielectrics

Photosensitive polymeric materials acting as positive photoresists were investigated for potential use as low k dielectrics at temperatures below 150^{o} C. In particular, Polyhedral Oligomeric Silsesquioxane containing, partially fluorinated copolymers (POSS-F), synthesized at IMEL, were tested as basic components of polymeric low-k insulators. The new materials, which contained also photoacid generators to allow lithographic patterning, were compared with conventional spin-on glasses (SOGs), with respect to their handling (application, curing, mechanical strength, patterning) and dielectric constant. It has been shown that the POSS-F materials present considerable advantages (related to the value of k and to handling) for use in Cu/low-k interconnects compared with SOGs cured at low temperatures.

Development of lithographic materials and processes for biological patterning

Our research program (in collaboration with the Institute of Radioisotopes and Radiodiagnostic Products with the support of EU project “Microprotein”) for novel lithographic materials and processes aiming at biomolecule patterning was continued.

New material options for resists suitable for multi-biomolecule patterning under biocompatible conditions were investigated. The usefulness of PEG macromonomers in the synthesis of copolymers used as components of such resists was proved (P. Economou, MSc thesis). Resist processes for patterning thiol SAMs (self assembled monolayers) on gold were also developed and used in the fabrication of sensors for electrochemical applications in collaboration with Krejci Eng (Czech Republic).

Task 3 Understanding Polymer Patterning Processes - Fundamental Physicochemical and Process Studies

Characterization (Physicochemical properties) of thin polymeric/resist films

For the realization of the 32nm and 32nm technology nodes the resist film thickness should be less than 100nm in order to fulfill the 3:1 aspect ratio criterion. The physicochemical properties of such thin polymeric/resist films deviate significantly from the bulk values. The conventional methodologies can not been applied in the case of thin films and thus new methodologies should be developed. In this field optical, based on multi wavelength interferometry, methodologies were developed for the monitoring of the glass transition temperature (fig. I.1.5a), and the dissolution. In both cases integrated set-ups (hardware and software (fig. I.1.5b)) were developed and successfully applied in the case of thin polymer/ resist (conventional and chemically amplified) resists. Those studies allowed the recommendation of specific recipes for the lithographic performance optimization. For example the effect of molecular weight on the critical thickness where the deviation of properties from the bulk ones is observed was revealed (fig. I.1.5c).

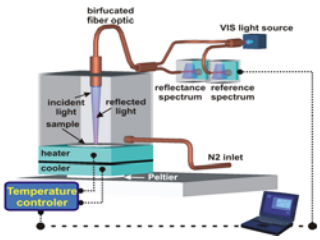


Fig. I.1.5a: *Schematic of the MWI experimental setup*

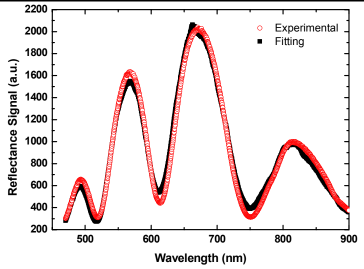


Fig I.1.5b: *A typical profile of the primary raw data from one temperature along with the results from the fitting procedure.*

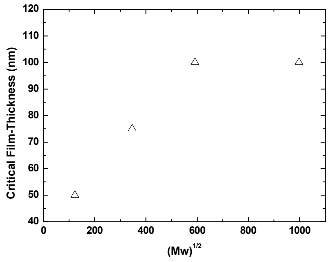


Fig. I.1.5c: *Critical film thickness for bulk properties, as a function of PMMA molecular weight*

SEM metrology

Discrimination and metrology results of microlithographic patterns from top-down SEM images were explored by means of morphological image analysis. The resulted images are segmented in order to derive a quality factor which discriminates the candidate images as under- or fully-developed. The proposed image analysis methodology achieves successful off-line discrimination between under-developed and fully-developed cases. For the latter case, the measuring method relies upon the evaluation of the connected regions in the SEM image after segmentation. This is expressed by the Useful Threshold Range (UTR), which corresponds to that specific value of connected regions obtained for the wider range of the threshold. In addition, the evaluated critical pattern parameters (CD, roughness) are found in good agreement to those derived from on-line procedures.

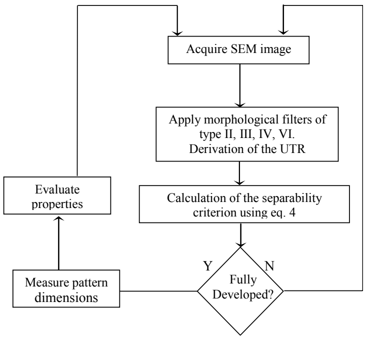


Fig. I.1.6a: *Flowchart of the metrology procedure*

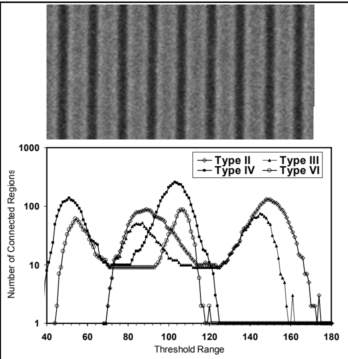


Fig. I.1.6b: *Original SEM image and corresponding plots of connected regions vs. threshold after filtering. Case of under-developed pattern*

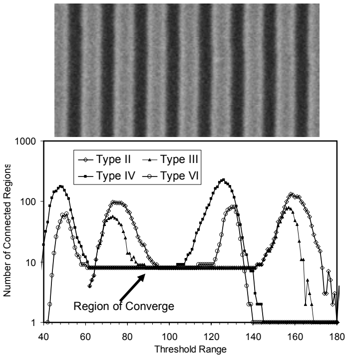


Fig. I.1.6c: *Original SEM image and corresponding plots of connected regions vs. threshold after filtering. Case of fully-developed pattern*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS

1. “Proton beam micromachining on strippable aqueous base developable negative resist”, I.Rajta E.Baradacs, M.Chatzichristidi, E.S.Valamontes, I.Uzonyi, I.Raptis, Nucl. Instrum. Meth. B 231 423(2005),
2. “Imprint lithography on poly(2-hydroxyethyl methacrylate), (PHEMA), and epoxydised novolac, (EPN) polymers”, F.A.Zacharatos, A.Olziersky, I.Raptis, E.Hristoforou, J. Optoelectron. Adv. Mater. 7 1121(2005)
3. “Fabrication and characterization of magnetically hard CoPt ordered sub-micron structures”, L.Castaldi, I.Raptis, E.Manios, D.Niarchos, J. Optoelectron. Adv. Mater. 7 1605(2005)
4. “Composition effects in polymer blends spin-cast on patterned substrates”, J.Raczkowska, P.Cyganik, A.Budkowski, A.Bernasik, J.Rysz, I.Raptis, P.Czuba, K.Kowalski, , Macromolecules 38 8486(2005)
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1. “Photochemically Induced Emission Tuning of Conductive Polymeric Materials used in OLEDs”, M. Vasilopoulou, G. Pistolis, and P. Argitis, J. of Physics, Conference Series, 10, 2005, 285.
2. “Characterization of various low-k dielectrics for possible use in applications at temperatures below 160 ^{o}C”, M. Vasilopoulou, S. Tsevas, P. Argitis and D. Kouvatsos, Journal of Physics, Conference Series, 10, 2005, 218.
3. “Fabrication of WO_3 –based electrochromic displays using solid or gel-like organic electrolytes”, M. Vasilopoulou, G. Aspiotis, P. Argitis and D. Davazoglou, Journal of Physics, Conference Series, 10, 2005, 329.
4. “Dissolution properties of ultrathin photoresist films with multiwavelength interferometry”, A. Kokkinis, E.S. Valamontes, I. Raptis, Journal of Physics: Conference Series 10, 2005 401

CONFERENCE PARTICIPATION

1. “Photochemically Induced Emission Tuning of OLEDs for Display and White Light applications”, M.Vasilopoulou, G. Pistolis, D. Georgiadou, D. Dimotikalli and P. Argitis, International Conference on Organic Electronics, Eindhoven, 21-23 June 2005.
2. “Protonic methacrylate polymeric electrolytes for all-solid-state WO_3-based electrochromic displays”, Vasilopoulou, I. Raptis, P Argitis, G. Aspiotis and D Davazoglou, MNE conference, Vienna, September 2005.
3. “Characterization of MOS diodes fabricated using sputter-deposited W or Cu/W films”, S. Tsevas, M. Vasilopoulou, D. Kouvatsos, T. Speliotis and D. Niarchos, MNE conference, Vienna, September 2005.
4. “Photochemically Induced Emission Tuning of Polymers used in OLEDs”,M.Vasilopoulou, P. Argitis, G. Pistolis, N. Stathopoulos, M. Rangoussi, 2nd International Scientific Conference in Information Technology and Quality,Spetses, 4 June 2005.
5. “Layer by layer UV microlithography for the fabrication of embedded microchannels”, M. Kitsara, M.Chatzichristidi, D.Niakoula, D.Goustouridis, K.Beltsios, P.Argitis, I.Raptis, Micro & Nano Engineering 2005 Conf. (Vienna, Austria, 09/2005)
6. “Electron beam lithography simulation for the fabrication of EUV masks”, G.P.Patsis, N.Tsikrikas, I.Raptis, N.Glezos, Micro & Nano Engineering 2005 Conf. (Vienna, Austria, 09/2005)
7. “Thickness-dependent glass transition temperature of thin resist films for high resolution lithography”, S.Marceau, J.-H.Tortai, J.Tillier, N.Vourdas, E.Gogolides, I.Raptis, K.Beltsios, K.van Werden, Micro & Nano Engineering 2005 Conf. (Vienna, Austria, 09/2005)
8. “Modelling of resist exposure and development for optimization of sub-quarter-micron patterns”, K.Vutova, G.Mladenov, T.Tanaka, K.Kawabata, I.Raptis, Micro & Nano Engineering 2005 Conf. (Vienna, Austria, 09/2005)
9. “Polycarbocycle-based molecular resists for EUV lithography”, D. Niakoula, P. Argitis, I. Raptis, E. Gogolides, V. P. Vidali, E. A. Couladouros, Wang Yueh, Janette Roberts, Robert Meagley, Int. Sematech EUVL symposium, November 2005, San Diego,USA.
10. “Photoresists based on (meth)acrylate copolymers and multistep lithographic process for the fabrication of submicron biomolecule microarrays”, M. Chatzichristidi, P. Oikonomou, A. Douvas, K.

Misiakos, I. Raptis, C.D. Diakoumakos, P. Argitis, P.S. Petrou, S.E. Kakabakos, ACS Pacific Polymer Conference, Maui, Hawai, USA, December 11-14, 2005

11. "Off line metrology on SEM images using gray scale morphology", E.N.Zois, I.Raptis, V.Anastassopoulos EMAS conference (Florence, Italy, 05/2005)
12. "Material and processing effects on the dissolution properties of thin resist films for high resolution lithography", A.Kokkinis, D.Goustouridis, E.S.Valamontes, I.Raptis, 5th Int. Conf. Polymer Surface Modification (06/2005, Toronto, Canada)
13. "Evaluation of optical methods for the glass transition temperature measurement of thin polymeric films", N.Vourdas, G.Karadimos, E.Gogolides, A.G.Boudouvis, I.Raptis, 4th Int. Conf. Instrumental Methods of Analysis (Iraklion, Greece, 10/2005)

INVITED TALKS-PRESENTATIONS

1. P. Argitis, Biological nanopatterning, Workshop on nanopatterning for advanced micro-arrays and biochips, N2L NoE, Muenster, March 4, 2005
2. P. Argitis, Polycarbocycle based molecular photoresists for EUVL, Third European EUVL workshop, Vienna, Austria, 18-19 September 2005
3. Invited Poster : D. Niakoula, P. Argitis, et al., Micro and Nano Engineering Conference 2005, Vienna, Austria, 20-22, September 2005

MSc THESES

1. "Material and processing effects on the dissolution properties of thin resist films for high resolution lithography", A.Kokkinis, (Graduate Program in Microelectronics, Dep. of Informatics, Univ, of Athens), Supervisor: I. Raptis
2. "Evaluation of (meth)acrylate copolymers as basic components of photoresists for deep UV lithography and fabrication of bio-microsystems", P. Economou, (Polymer Science and Applications Graduate Program, Dep. of Chemistry, Univ. of Athens), Supervisor : P. Argitis
3. "Imprint lithography on poly (methyl methacrylate materials)", F.A. Zacharatos, Nat. Techn. Univ of Athens, Supervisors : I. Raptis, E.Histoforou

DIPLOMA THESES

1. "Glass transition monitoring of thin polymeric films", G.Karadimos, Departm. of Materials Science and Eng., University of Ioannina, Supervisor: I.Raptis
2. "Photochemically induced emission tuning of organic light emission diodes", D. Georgiadou, Department of Chem. Engineering, National Technical University of Athens, Assoc. Prof. D. Dimotikali, Supervisors : M. Vasilopoulou, P. Argitis

PATENTS GRANTED

1. "Polycarbocyclic derivatives for modification of resist optical and Etch resistance properties", E. Gogolides, P. Argitis, E. Couladouros, V. Vidali, M. Vasilopoulou, G. Cordoyanis, EP Patent 02790329.3.

PATENT APPLICATIONS

1. "Molecular resists based on functionalized polycarbocycles", P. Argitis, E. Gogolides, D. Niakoula, V. P. Vidali, E. Couladouros, D. Gautan, Greek patent appl. (OBI), September 2005

Project I. 2: LITHOGRAPHY and PLASMA PROCESSES

Project leader: Dr E. Gogolides

Key researchers: Dr E. Gogolides, Dr A. Tserepi

Collaborating researchers: Dr K. Misiakos, Dr P. Argitis, Dr I. Raptis

Post-doctorals: Dr G. Patsis, Dr V. Constantoudis, Dr G. Kokkoris

PhD candidates: P. Bayiati, N. Vourdas

External collaborators: Prof. A. Boudouvis (NTUA), Dr P. Leunissen (IMEC), Prof. Th. Christopoulos (U. Patras), Y. Wang, J. Roberts (INTEL), Dr S. Kakabakos (IRRP, NCSR-Demokritos), Dr P. Petrou (IRRP, NCSR-Demokritos)

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- EU IST-STREP SOARING, Contract N^o 35254, 1/3/2004-28/1/2005
- Contract with the company INTEL- Mol-EU, 1/5/2003-30/4/2006
- EU NMP NoE Nano2Life, Contract N^o 500057, 1/2/2004-31/2/2008
- GSRT, PENED 03 ED 202, 1/12/2005-31/11/2008

Research orientation:

Our work in nanolithography focused on metrology and simulation of Line Edge Roughness, a side effect of the nanoscale era, which has deleterious effects on transistor operation. We have developed a protocol and software for LER measurement from SEM images. In addition, we are improving a stochastic nanolithography simulator to design processes with minimal LER. This work is in strong collaboration with IMEC and INTEL.

Microfluidics fabrication and actuation has consumed significant effort. A platform technology based on soft lithography has been complemented with sealing processes used for fabrication of microfluidic devices. We are also proposing an alternative technology for microfluidics patterned on polymeric substrates using plasma etching and plasma functionalisation. First results have been achieved on plexiglass. Selective plasma deposition of polymers has been used to create open channel microfluidics actuated with electrowetting. We demonstrated movement of protein solutions without protein loss on the surface.

Nanotexturing of polymers with plasmas has produced impressive results for PDMS where nanocolumns were created and superhydrophobicity was demonstrated. A patent was filed and applications on Microfluidics are being designed. Nanotexturing and nanoroughness creation from plasmas is being probed with Monte Carlo simulations.

Finally, topography evolution during plasma etching was investigated for deep silicon etching using our Integrated Plasma Topography Evolution Simulator in order to achieve very high aspect ratios and propose parameter ramping strategies. This work is significant for MEMS fabrication.

Main results in 2005

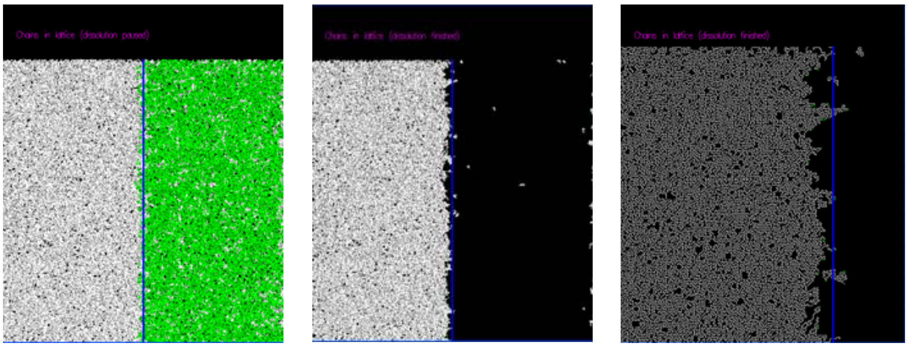
The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Nanopatterning: Metrology and simulation of Line Edge Roughness (LER)

a. *Simulation of lithography for LER reduction*

G. Patsis, E. Gogolides

Resolution and line edge roughness are related to the used polymer chain size. They can further be strongly affected by acid diffusion and processing. It is thus essential to guide appropriate material design choices using simulations taking into account all relevant processing steps. Stochastic Monte Carlo techniques are used with a quasi-static dissolution algorithm to simulate dissolution of polymer lattice based on the concept of critical ionisation. Etching is simulated by applying an isotropic deformation on a numerically obtained line edge.LER decreases with decreasing polymerization length when acid diffusion is small. Otherwise, acid diffusion tends to result in lower LER for longer polymers. LER can be reduced during pattering. For shorter diffusion length the decrease in LER is initially much larger. The reduction in LER is related to the spatial frequency components of the resist.



(a) (b) (c)

Fig. I.2.1: *Simulation of the dissolution of a thin polymer layer and LER formation (a) unexposed (left) and exposed (right) polymer chain lattice (b) the same lattice as in (a) after exposed polymer dissolution (c)magnification of the edge to observe roughness.*

b. *Metrological software for LER analysis*

V. Constantoudis, G. Patsis, E. Gogolides

A software has been developed for the analysis of SEM images during the years 2003-04. During 2005 the software has been expanded and standardized to become a tool for LER measurement and comparison of various lithographic materials. Software demos are in use at IMEC, INTEL and other research centers and companies. The protocol for LER/LWR resist comparison consists of the following steps:

1. Acquisition of top-down CD-SEM images of the resist line patterns to be analyzed.
2. Application of an off line image analysis algorithm with noise smoothing filter and extraction of the line edges of the images (see the top-left image of the output fig.).
3. Estimation of the height-height correlation function HHCF (top-right figure) and the three curves $\sigma_{LWR}(L)$, $CD_{variation}(L)$ (down-left), $rms_{sigma}(L)$ (down-right) from the obtained line morphologies and averaged over all available resist lines and SEM images.
4. Calculation of the LWR descriptors used for resist comparison: a) the line length independent value of the line σ_{LWR} *(inf)* calculated by the relationship $\sigma_{LWR}{}^2(inf) = \sigma_{LWR}{}^2(L) + CD_{variation}{}^2(L)$, b) *correlation length* ξ after which the line looks flat or the sigma correlation length L_S after which the σ_{LWR} does not depend strongly on the length of the measurement box, and c) *roughness exponent* α which gives the relative importance of high frequency fluctuations on LWR and thus determines how fast the sigma drops off as the measured length decreases.

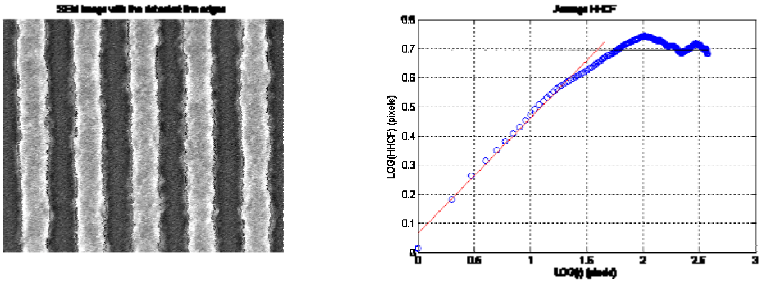


Fig. I.2.2: *The figures-output of the software*

Task 2 Microfluidics fabrication and actuation using plasma processes

a. *Plasma etching for fabrication of PMMA Microfluidic devices*

N. Vourdas, E. Gogolides

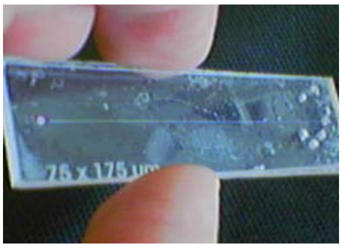


Fig. I.2.3:
Microfluidic channel made on PMMA by means of direct plasma etching. Patterning and surface properties control are performed simultaneously.

The fabrication of microfluidic devices with features of 10-1000μm size are of great importance in many fields of analytical science, where a small quantity of sample is available, enhanced resolution and sensitivity in separation is needed and increased functional integration is desired (medical, chemical and biochemical analysis, microchemistry etc). Even though the first microfluidic devices were fabricated on silicon and glass, the need for easy fabrication, low cost and disposability has recently shifted the attention on polymeric materials.

We demonstrated an alternative method for fabrication of microfluidic devices based on direct O_2 plasma etching of polymers -PMMA in particular- using a photosensitive silicon-containing polymeric mask (poly-dimethylsiloxane-PDMS). Both patterning and surface properties control is attained simultaneously according to specific analysis requirements.

b. *Plasma deposited films for electrowetting-based actuation in microfluidics*

P. Bayiati, A. Tserepi, K. Misiakos

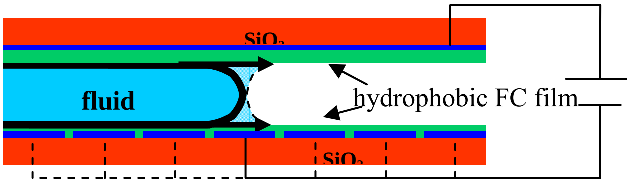


Fig. I.2.4: *Microfluidic device and fluid transport based on electrowetting*

This work focuses on the plasma deposition of fluorocarbon films on electrodes, in order to obtain surfaces that can be varied from hydrophobic to hydrophilic with voltage application (electrowetting). Such films can be used for biological fluid transport in microfluidic devices actuated by voltage application (fig. I.2.4).

Fluorocarbon films with appropriate surface properties (small hysteresis) were deposited in fluorocarbon plasmas (C_4F_8). Composite films (plasma-deposited fluorocarbon films on Si_3N_4 films) were mainly used for the improvement of the dielectric properties of the stack-structure and its use in reversible electrowetting (fig. I.2.5). Electrowetting experiments were conducted using protein solutions for investigating the conditions under which transport of protein solutions is feasible. Furthermore, an open microfluidic device was fabricated and protein solution transport was demonstrated on devices under appropriate conditions.

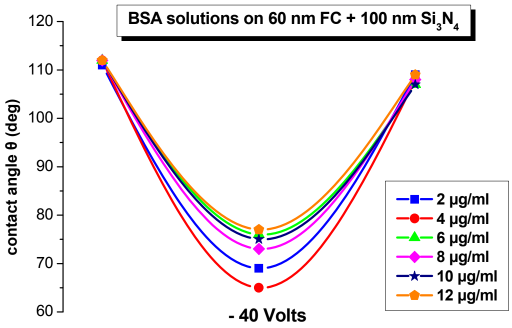


Fig. I.2.5: *Reversible electrowetting using protein solutions on composite (plasma-FC deposited on Si_3N_4) materials.*

c. *Fabrication technologies for microfluidic devices based on soft lithography*

M. Vlachopoulou, P. Bey, A. Tserepi, K. Misiakos

The process of replica molding (soft lithography) based on the lithography of SU(8) for the fabrication of the mold has been adopted for the rapid prototyping of PDMS-based microfluidic devices. The lithography of SU(8) has been used for the fabrication of dual-height structures in SU(8) such as those shown in fig. I.2.6 and thus it offers the capability for simultaneous fabrication of both open and closed channels in PDMS (fig. I.2.7). For fabrication of closed microchannels on PDMS, sealing procedures have been developed for non-irreversible and/or irreversible sealing with materials such as PDMS, glass, plexiglass, and Polystyrene. Microfluidic devices have been fabricated, with the addition of interfaces with external tubing for inlet and outlet of the reagents, such as the one shown in fig. I.2.8. A microfluidic module is shown in the picture, with a red dye flowing through it for demonstration purposes. A similar microfluidic module is used for bio-spotting when placed on an optoelectronic bio-sensor (see PIII-2).

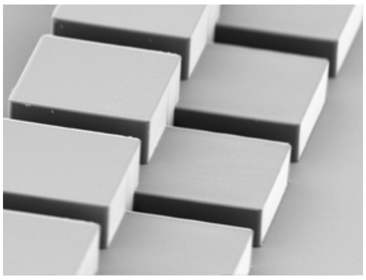


Fig. I.2.6: *A dual-height structure fabricated by double photolithography of SU(8). Structures 30 and 60 μm high are shown.*

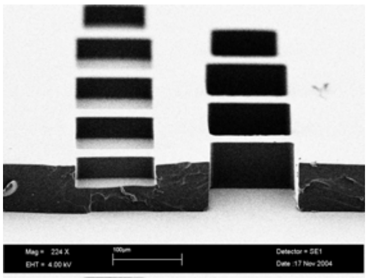


Fig. I.2.7: *30 and 60-μm deep structures fabricated by replica molding of PDMS (using as a mold an SU(8) structure similar to that in fig. I.2.6).*

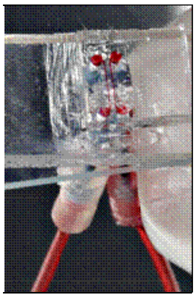


Fig. I.2.8: *A microfluidic device in PDMS supported on plexiglass and bearing two microchannels indicated by the red dye flowing through.*

Task 3 Plasma nanostructuring-nanotexturing of polymers

a. Design and Control of Surface Wetting properties of PDMS by plasma processing

M. Vlahopoulou, K. Tsougeni, A. Tserepi, E. Gogolides

Poly-dimethyl siloxane (PDMS) is a material widely used in soft lithography techniques for the fabrication of soft stamps, molds, and as a structural material for microfluidic devices. In all of these applications, control of the surface topography and the resulting wetting properties is greatly desired, as it can potentially affect the functionality of the structure/device.

In our work, the effect of O_2 and SF_6 plasma treatments on (commercial elastomer Sylguard 184) PDMS surfaces is investigated due to the use of the former for the activation of PDMS surfaces before channel sealing in microfluidic device fabrication, while the use of the latter for plasma-based patterning of PDMS devices. Both treatments were found to significantly affect the surface topography of PDMS (in addition to its surface chemistry).

In specific, surface undulations were observed after O_2 plasma treatments (fig. I.2.9), of random orientation but with periodicity of rms in the nanoscale and wavelength in the range 200-600 nm, depending on treatment duration. After ion-induced dominated treatments in SF_6 plasmas, columnar-like structures (fig. I.2.10 and I.2.11) appear on the PDMS surface, with pillar diameter in the order of 100 nm and with height increasing linearly with the duration of plasma processing. In both cases, when FC deposition on the modified PDMS surface follows plasma treatment, increased water contact angles (140°-150°) were observed (fig. I.2.12). Water contact angles on surfaces of topography similar to those shown in fig. I.2.9 indicate Wenzel type surfaces characterized by high hysteresis, while contact angles on surfaces of topography similar to that shown in fig. I.2.10, I.2.11 indicate surfaces in the Cassie-Baxter regime (minimal hysteresis, and thus of minimal friction against droplet motion).

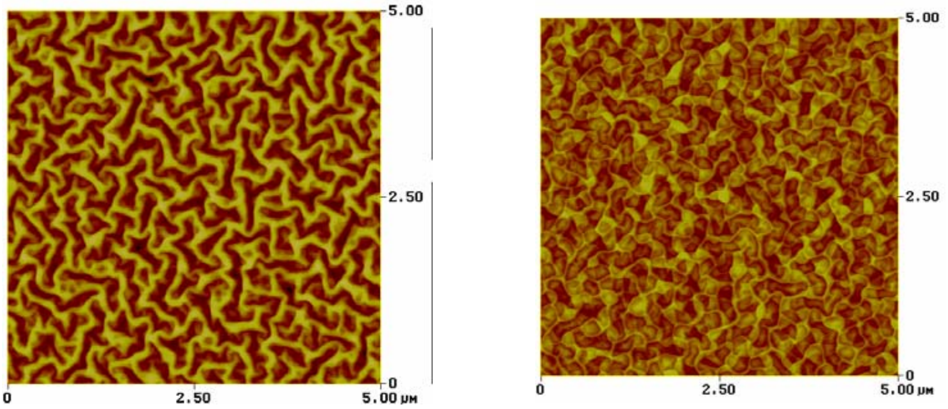


Fig. I.2.9: *AFM top view image of a PDMS surface after (a) 4 and (b) 10 min treatment in O_2 plasma. Roughness analysis gave an rms value of (a) 46 nm and a periodicity of 324 nm and in (b) an rms value of 28 nm and a periodicity of 461 nm*

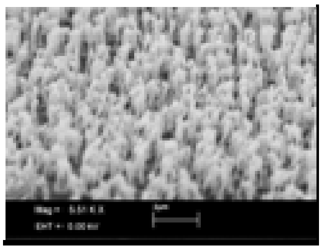


Fig. I.2.10: *SEM image of a tilted PDMS surface after 6 min treatment in SF_6 plasmas*

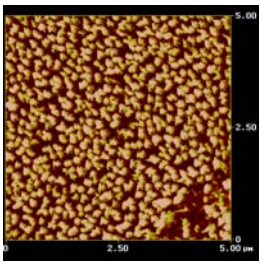


Fig. I.2.11: *Top-down AFM image of a PDMS surface after 2 min treatment in SF_6 plasmas*

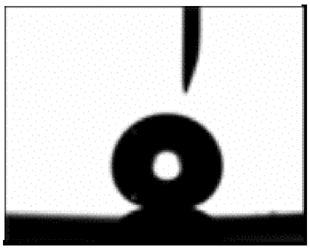


Fig. I.2.12: *Enhanced contact angle (150°) on a plasma-treated PDMS surface*

Task 4 Simulation of micro and nano-structuring evolution from plasma processes

a. *Deep silicon etching*

G. Kokkoris, P. Papasimakis, E. Gogolides, A. Tserepi

The spread of microelectromechanical systems (MEMS) application to diverse industries (e.g. automotive, aerospace, bio-medical, computer peripherals and telecommunications) poses several and different demands in the construction of the building blocks of MEMS. A common and key requirement in MEMS fabrication is the capability of making silicon structures with high aspect ratio (ratio of the depth to the width of the structure). The Bosch process, a multiple step etching process, including successive etching and deposition steps, is the most common one used to construct deep silicon structures.

An integrated simulation framework for topography evolution during plasma etching of structures consisting of three modules a) a flux calculator module, b) surface etch module and c) a topography evolution algorithm is applied in the Bosch process. The theoretical study has been complemented with experiments to a) define the parameters and coefficients of the surface models required and b) develop a recipe for high aspect ratio and anisotropic etching, i.e. the so-called parameter ramping.

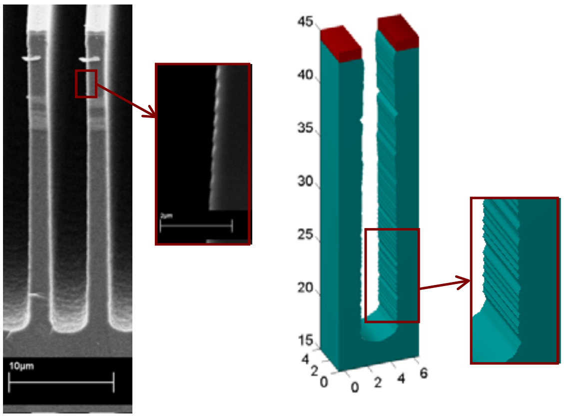


Fig. I.2.13: *Experimental and simulation results of etching Si trenches with the Bosch process.*

b. *Monte Carlo simulation of roughness formation during plasma etching*

V. Constantoudis, G. Kokkoris, E. Gogolides

The aim of this research activity is to understand and control the formation of surfaces roughness on Si and polymer films during plasma etching by developing kinetic Monte Carlo simulation algorithms. Simulation algorithms considering both anisotropic etching by ions and isotropic etching by neutrals have been developed in both (1+1) and (2+1) dimensions.These algorithms have been used for the explanation of the experimentally observed behaviour in plasma etched Si films consisting of the linear increase of roughness with etching time and the occurrence of columnar surface structures that are diluted and widened with time. We have found that the inclusion in the etching process of the simultaneous isotropic deposition of etching resistant particles forming a local nano-masking on the film is able to explain the experimentally observed roughness morphology (fig. I.2.14). Further, we have addressed the influence of the reflection of ions and the isotropic etching by neutrals on roughness formation.

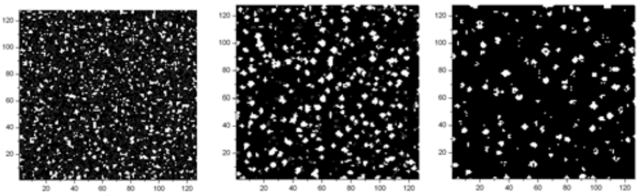


Fig. I.2.14a: *Si Surface morphology vs etching time as given by Monte Carlo simulation*

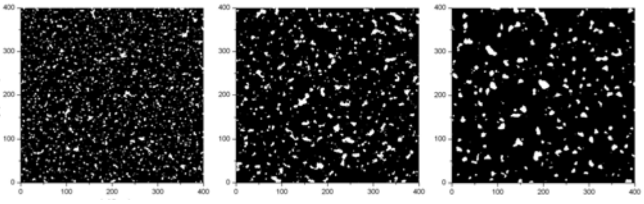


Fig. I.2.14b: *Experimental Si surface morphology vs etching time.*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. “Fractal roughness of polymers after lithographic processing”, Constantoudis, V., Gogolides, E., Patsis, G.P., Sarris, V., Tserepi, A., Diakoumakos, C., Valamontes, E.S., (2005) Japanese Journal of Applied Physics, Part 2: Letters, 44 (1-7), Pages L186-L189.
2. “Increased plasma etch resistance of thin polymeric and photoresist films”, Vourdas, N., Boudouvis, A.G., Gogolides, E., (2005) Microelectronic Engineering, 78-79 (1-4), Pages 474-478.
3. “Monte Carlo study of surface and line-width roughness of resist film surfaces during dissolution”**,** Patsis, G.P., (2005) Mathematics and Computers in Simulation*,* 68 (2), Pages 145-156.
4. “Stochastic simulation of thin photoresist film dissolution: A dynamic and a quasi-static dissolution algorithm for the simulation of surface and line-edge roughness formation”, Patsis, G.P., (2005) Polymer, 46 (7), Pages 2404-2417.
5. “Determining the impact of statistical fluctuations on resist line edge roughness”, Leunissen, L.H.A., Ercken, M., Patsis, G.P., (2005) Microelectr. Engineering, 78-79 (1-4), Pages 2-10. Cited 3 times.
6. “Tailoring the surface topography and wetting properties of oxygen-plasma treated polydimethylsiloxane”**,** Tserepi, A., Gogolides, E., Tsougeni, K., Constantoudis, V., Valamontes, E.S., (2005) Journal of Applied Physics, 98 (11), Pages 1-6.
7. “A Stochastic Photoresist-Polymer Dissolution Model Combining the Percolation and Critical Ionization Models”**,** V. Sarris, G. P. Patsis, V. Constantoudis, A. G. Boudouvis and E. Gogolides, (2005) Japanese Journal of Applied Physics, Part 2: Letters, 44 (10), Pages 7400-7403.
8. “Material and process effects on line-edge-roughness of photoresists probed with a fast stochastic lithography simulator”**,** G. P. Patsis & E. Gogolides, J. Vac. Sci. Technol. B 23(4), 1371, Jul/Aug 2005

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Patterning of thick polymeric substrates for the fabrication of microfluidic devices”, Vlachopoulou, M.E., Tserepi, A., Vourdas, N., Gogolides, E., Misiakos, K., (2005) *Journal* of Physics: Conference Series, 10 (1), Pages 293-296.
2. “Characterization and modeling of Line Width Roughness (LWR)”, Constantoudis, V., Gogolides, E., Roberts, J., Stowers, J.K., (2005) Progress in Biomedical Optics and Imaging - Proceedings of SPIE*,* 5752 (III), Pages 1227-1236.
3. “Plasma etch rate measurements of thin PMMA films and correlation with the glass transition temperature”, Vourdas, N., Boudouvis, A.G., Gogolides, E., (2005) *Journal of* Physics: Conference Series, 10 (1), Pages 405-408.
4. “Effects of model polymer chain architectures of photo-resists on line-edge-roughness: Monte Carlo simulations”, Patsis, G.P., Gogolides, E., (2005) J. of Physics: Conf. Series*,* 10 (1), Pages 389-392.
5. “Characterization and Modeling of Line Width Roughness (LWR)”, V. Constantoudis, E. Gogolides, (2005) Proceedings of SPIE, v. 5752 (3), pages 1227-1236
6. “Electron-beam lithography simulation for EUV mask applications”, Patsis, G.P., Glezos, N., (2005) Journal of Physics: Conference Series*,* 10 (1), Pages 385-388
7. “Plasma Etching Fabrication Of Pmma-Based Microfluidic Devices For Bioanalytical Applications”, N. Vourdas, A. Tsougeni, A. Tserepi, A.G. Boudouvis and E. Gogolides, S. Tragoulias, T.K. Christopoulos, In Proceedings of 17th International Symposium on Plasma Chemistry (ISPC) (CD vesion, Nr.693_Vourdas et al(1)), Toronto-Canada, August 7-11, 2005, R. D’ Agostino et al, Eds.
8. “Effects of model polymer chain architectures on the self-affine-characteristics of dissolving photopolymer films”, G .P. Patsis, N. Tsikrikas, E. Gogolides, In Proceedings of 3rd International Symposium on Nanofacturing (ISNM), (CD version, TMP3), Limassol-Cyprus, November 3-5, 2005
9. “Combined Metrology and Simulation of imprinted photopolymer lines/ spaces. Extraction of Line-Edge roughnessdescriptors”, G.P. Patsis, N. Tsikrikas, V. Constantoudis, E. Gogolides, In Proceedings of 3rd International Symposium on Nanofacturing (ISNM), (CD version, TAA4), Limassol-Cyprus, November 3-5, 2005
10. “Mechanisms of Nano-Roughness Formation on Plasma Etched surfaces” , V. Constantoudis, A. Tserepi, G. Boulousis, P. Papasimakis, E. Gogolides, In Proceedings of 3rd International Symposium on Nanofacturing (ISNM), (CD version, FMB2), Limassol-Cyprus, November 3-5, 2005
11. “Design of PDMS surfaces with controlled nano-texturing and wettability”, A. Tserepi, K. Tsougeni, G. Boulousis, V. Constantoudis, E. Gogolides, In Proceedings of 3rd International Symposium on Nanofacturing (ISNM), (CD version, FAA1) Limassol-Cyprus, November 3-5, 2005
12. “Plasma Treatment Of Polymers For Bioanalytics”, (in greek) N. Vourdas, A. Tserepi, M. Vlachopoulou, E.Gogolides, In Proceedings of 2nd Panhellenic Conference on Plastics (CD-version, neestexnologies 15), Athens, 20-21 March, 2005, K. Papaspyrides et al. Eds.
13. “New Nanocomposite materials. Thermomechanical characterization and morphology studies after O_2 plasma treatment”, (in greek) S.I. Marras, I. Zoubourtikoudis, N. Vourdas, V. Constandoudis, A. Tserepi, E. Gogolides, C. Panagiotou, In Proceedings of 2nd Panhellenic Conference on Plastics (CD-version, neaylika 32), Athens, 20-21 March, 2005, K. Papaspyrides et al. Eds.

INVITED TALKS

1. In MNE 2005:E. Gogolides, V. Constantoudis, G.P. Patsis, A. Tserepi, “Line Edge nano-roughness nad surface nano-texture resulting fron patterning processes: A blessing or a curse?”
2. SEMATECH Workshop on Resist Line Edge Roughness (27th February 2005)
   E. Gogolides, V. Constantoudis, G.P. Patsis, « Metrology – Characterization and Simulation of Line Edge Roughness »

CONFERENCE PRESENTATIONS

Presentations in MNE 2005:

1. “Molecular resists based on novel polycarbocycle derivatives”, D. Niakoula, P. Argitis, I. Raptis, E. Gogolides, V.P. Vidali, E.A. Couladouros, Wang Yueh, Janette Roberts, Robert Meagley
2. “Effects of model polymer chain architectures and molecular weight of photoresists on line-edge roughness. Monte Carlo Simulations”, G.P. Patsis, E. Gogolides
3. “Micro- and nano-structuring of polydimethylsiloxane for production of super-hydrophobic surfaces”, M.E. Vlachopoulou, A. Tserepi, P. Bayiati, E. Gogolide
4. “Monolithic silicon optoelectronic transducers and elastomeric fluidic modules for bio-spotting and bio-assay experiments”, K. Misiakos, P.S. Petrou, S.E. Kakabakos, M.E. Vlachopoulou, A. Tserepi, E. Gogolides, H.H. Ruf
5. “Line Edge nano-roughness nad surface nano-texture resulting fron patterning processes: A blessing or a curse?”, E. Gogolides, V. Constantoudis, G.P. Patsis, A. Tserepi
6. “Material and processing impact on thermal propeties of thin resist films for high resolution lithography”, J.H. Tortai, S. Marceau, G. Karadimos, N. Vourdas, E. Gogolides, I. Raptis, K. van Werden
7. “Alternative micro-hotplate design for low power sensor arrays”, R. Triantafyllopoulou, S. Chatzandroulis, C. Tsamis, A. Tserepi
8. “Simulation of deep etching of silicon structures for MEMS fabrication”, G. Kokkoris, P. Papassimakis, E. Gogolides, and A. Tserepi, International Conference on micro and nano-Engineering (MNE) 2005, Vienna, Austria, September 19-22.

Presentations in ISNM 2005:

9. “Effects of model polymer chain architectures on the self-affine-characteristics of dissolving photopolymer films”, G.P. Patsis, N. Tsikrikas, E. Gogolides
10. “Combined Metrology and Simulation of imprinted photopolymer lines/ spaces. Extraction of Line-Edge roughnessdescriptors”, G.P. Patsis, N. Tsikrikas, V. Constantoudis, E. Gogolides
11. “Mechanisms of Nano-Roughness Formation on Plasma Etched surfaces”, V. Constantoudis, A. Tserepi, G. Boulousis, P. Papasimakis, E. Gogolides,
12. “Design of PDMS surfaces with controlled nano-texturing and wettability”, A. Tserepi, K. Tsougeni, G. Boulousis, V. Constantoudis, E. Gogolides

Presentations in SPIE 2005:

13. “Characterization and Modeling of Line Width Roughness (LWR)”, V. Constantoudis, E. Gogolides, J.K. Stowers and J. Roberts,

Presentations in CIP (15th International Colloqium on Plasma Processes) 2005

14. “Simulation of deep reactive ion etching of silicon (Bosch process)”, G. Kokkoris, P. Papassimakis, E. Gogolides, and A. Tserepi, 15th International Colloquium on Plasma Processes (CIP 05), Grenoble, France, June 6 – 9, 2005.
15. “Mechanisms of roughness formation during plasma etching”,V. Constantoudis, G. Kokkoris, A. Tserepi, and E. Gogolides, 15th International Colloquium on Plasma Processes (CIP 05), Grenoble, France, June 6 – 9, 2005.

Presentations in ISPC 2005:

16. “Plasma Etching Fabrication Of Pmma-Based Microfluidic Devices For Bioanalytical Applications”, N. Vourdas, A. Tsougeni, A. Tserepi, A.G. Boudouvis and E. Gogolides, S. Tragoulias, T.K. Christopoulos, In Proceedings of 17th International Symposium on Plasma Chemistry (ISPC) (CD), Toronto-Canada, August 7-11, 2005, R. D’ Agostino et al, Eds.

Presentations in 2nd Panhellenic Conference on Plastics (in greek):

17. “Plasma Treatment Of Polymers For Bioanalytics”, (in greek) N. Vourdas, A. Tserepi, M. Vlachopoulou, E.Gogolides, In Proceedings of 2nd Panhellenic Conference on Plastics (CD-version), Athens, 20-21 March, 2005, K. Papaspyrides et al. Eds.
18. “New Nanocomposite materials. Thermomechanical characterization and morphology studies after O2 plasma treatment”, (in greek) S.I. Marras, I. Zoubourtikoudis, N. Vourdas, V. Constandoudis, A. Tserepi, E. Gogolides, C. Panagiotou, In Proceedings of 2nd Panhellenic Conference on Plastics (CD-version), Athens, 20-21 March, 2005, K. Papaspyrides et al. Eds.

Presentation in “Dynamics Days Conference” Berlin, July 2005.

19. “Fractal structures in nanoelectronics”, V. Constantoudis , G.P. Patsis, A.Tserepi, K.Tsougeni, G.Boulousis, E.Valamontes and E. Goggolides

Presentation in XXI Panhellenic Conference on Solid State Physics and Material Science

20. “Mechanisms of roughness formation during plasma etching “, V. Constantoudis, A. Tserepi, G. Boulousis, P. Papasimakis and E. Gogolides, XXI Panhellenic Conference on Solid Physics and Material Science, Nicosia, August 2005

Presentation in 1st Panhellenic Conference on Metrology

21. “Nanoscale Roughness measurements”, V. Constantoudis, G. Patsis, E. Gogolides, 1st Panhellenic Conference on Metrology, Athens, November 2005

Ph. D. theses

1. “Integrated simulation of topography evolution during plasma etching of micro and nanostructrures”, Kokkoris George

M. Sc theses

1. “Selective deposition of fluorocarbon films and application in protein arrays”, Matrozos Evrymahos
2. “Fabrication and simulation of microstructures by plasma processing”, Papassimakis Panagiotis
3. “Modification of PDMS surfaces in O2-based plasmas”, Tsougeni Ekaterene

Diploma theses

1. “Study of the lithographic process of wet silylation of epoxy polymers with emphasis in the effect of humidity”, Kontziabassis D.
2. “Fabrication technologies for plastic bio-microsystems”, Bey Pierre, (Academic Industrial Training (9 months) for the Diplome Universitaire d’ Etudes Technologiques Internationalles-IUT 1 Universite Joseph Fourier)

Laboratory Training

1. Summer School “Methods in Micro-Nano Technologyand Nanobiotechnology”,
   6-10 June 2005
   Laboratory courses:
   “Microfluidics with soft lithography” (A. Tserepi, M. Vlachopoulou)
   “Microfluidics with Plasma Etching” (E. Gogolides, N. Vourdas)

Patents granted

1. “Polycarbocyclic derivatives for modification of resist, optical and etch resistance properties” (E. Gogolides, P. Argitis, E. Kouladouros-PCT/EP/02/12284)
2. “Lithographic materials based on polymers containing polyhedraloligomeric silsesquioxanes” (E. Gogolides, P. Argitis, -PCT/Gr03/0018)

Patent applications

1. “Molecular resists based on polyarbocycles” (P. Argitis, E. Gogolides, E. Kouladouros-appl. no 20050100472/16.9.2005)
2. “Method for the fabrication of surfaces of high surface area ratio on polymer/ plastic substrates” (A. Tserepi, E. Gogolides, K. Misiakos-appl. no 20050100473/16.9.2005)

Project: I. 3: FRONT-END PROCESSES

Project leader: Dr C. Tsamis

Post-doctoral Scientists: Dr D. Skarlatos

PhD candidates: A. Chroneos, N. Kelaidis

Collaborating researchers from other projects: Dr P. Normand

External Collaborators: Prof. D. Tsoukalas (NTUA), Dr R. Grimes (Imperial College. UK), Dr V. Valamontes (TEI of Athens), Prof. Ph. Komninou (Univ. of Thessaloniki), Dr A. Claverie (CEMES), Dr F. Cristiano (LAAS)

Funding:

- GSRT-PENED-03ED496, “Dopant diffusion and activation in Group-IV semiconductors (Strained Silicon and Germanium) for novel nanoelectronic devices”, 1/11/2005-1/11/2008
- GSRT-Bilateral project NON-EU-204 (Greece-USA), Strained Si, 1/3/2006-28/2/2008

Research orientation:

- Study of dopant diffusion/activation and point/extended defect kinetics in Group-IV semiconductors (Silicon, Strained Silicon, Germanium) for CMOS applications
- Thermal processes for ultra-thin gate dielectrics (oxides, oxynitrides) in Group-IV semiconductors for CMOS applications
- Process optimization for Nanodevices (Fabrication, Electrical Characterization)
- Continuum and atomistic simulation of processes and devices

Main results in 2005

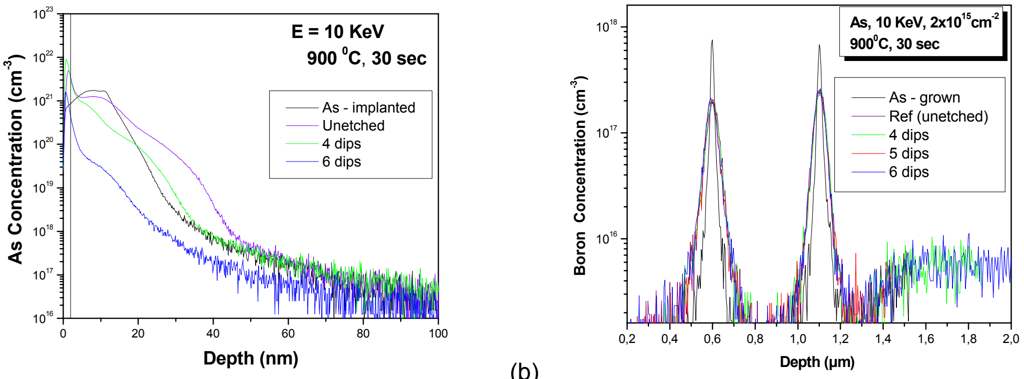
The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Dopant diffusion and defects in silicon

1.a *Arsenic diffusion in silicon*

C. Tsamis and D. Skarlatos

In this work we investigated arsenic diffusion and the interstitial injection caused by low-energy, high-dose arsenic implantation. The approach consisted in monitoring the diffusion both of arsenic, implanted with low energy, and of boron in buried δ-doped layers that exist below the implanted surface. Successive removal of Si implanted with arsenic is performed, using low temperature oxidation (<70°C), in order to control the total amount of damage that will influence the buried layer. Experimental results of arsenic and boron profiles indicate that the contribution of the implantation damage to the TED of arsenic and boron is not the main one. On the contrary, interstitial generation due to arsenic clustering seems to be more important for the present conditions. Theoretical studies and experimental evidence indicate that As clusters form around a vacancy with the consequent injection of silicon interstitials.



(a) (b)

***Fig. I.3.1:** Simultaneous arsenic **(a)** and boron **(b)** diffusion at 900^{0}C for 30 sec after controlled removal of the implantation damage by successive etching step of the silicon surface.*

1.b Extended defect formation and evolution under inert nitrided SiO_2/Si interfaces

D. Skarlatos, P. Tsouroutas and C. Tsamis

A systematic study of the dissolution kinetics of Dislocation Loops (DLs) in the vicinity of inert SiO_2/Si and nitrogen–rich SiO_2/Si interfaces (fig. I.3.2) was performed. The DL layer after its formation consisted of 10-20 % Frank DLs and 90-80 % perfect prismatic loops. Study of the differences of the kinetics between the two loop populations during in (N_2) ambient annealing as a function of the interface type showed that during the non-conservative Ostwald ripening process, the defects band loses interstitials mainly due to the dissolution of perfect prismatic loops, while Frank loops remain almost unaffected by the presence of both interfaces. In parallel a competition between the interface and the population of Frank loops in absorbing the interstitials released by the prismatic loops took place (fig. I.3.3). Analysis of the experimental results indicates that the nitrogen–rich SiO_2/Si interface is less effective interstitial sink than the common one interface and under specific annealing conditions less effective even than the small Frank loops population.

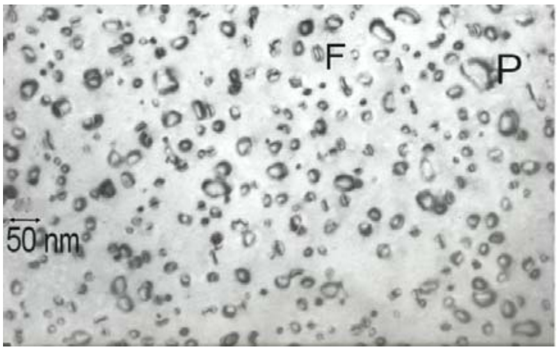


***Fig. I.3.2:** Representative TEM image of a dislocation loops band.*

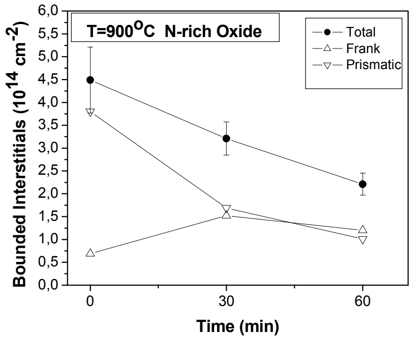


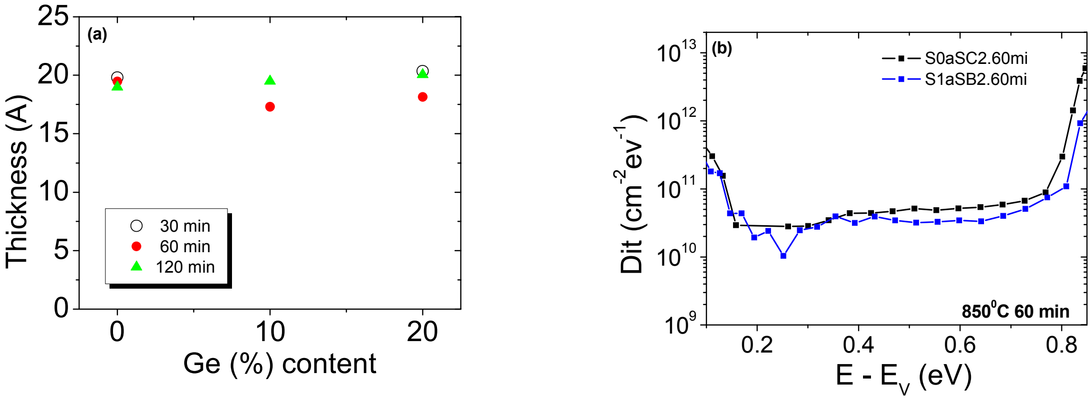
***Fig. I.3.3:** Variation of bounded interstitials within the dislocation loops band.*

Task 2 Ultra-thin oxide growth in Strained Silicon

N. Kelaidis, D.Skarlatos, V. Ioannou–Sougleridis and C. Tsamis

Integrated circuits industry has entered since years the nanoscale searching for alternative high carrier mobility substrates, which will enable the development of devices with enhanced performance as compared to those fabricated using the standard silicon technology. One of the most promising materials is Strained Silicon. As a consequence, the study of techniques of ultra-thin and highly reliable oxide formation on strained silicon substrates is of particular interest. Oxidation of nitrogen - implanted silicon is one of the methods developed in standard Silicon Technology that enables the formation of various oxide thicknesses across the silicon substrate using one single oxidation step, which is helpful for System-On-Chip fabrication.

In the present work we perform a systematic study of oxidation of very low energy nitrogen implanted strained silicon in terms of oxide growth, structural characterization of the implanted strained silicon substrates and the electrical properties of the ultrathin oxides as a function of the substrate strain level. It has been recently demonstrated by our group [*D. Skarlatos et al., JAP, 96(1)***,** *p.300-309, 2004*] that using very low implantation energy (<10 KeV) can result in the formation of ultrathin (<3.5 nm), highly reliable, nitrided oxides on defect–free silicon substrates. Nitrogen (N_2) was implanted in strained silicon substrates of various strain levels and oxidations were performed at various temperatures and times. It is shown that the oxidation rate, and as consequence nitrogen diffusion towards the surface, is independent on the substrate strain level. Detailed TEM analysis revealed the full absence of extended defects in the strained silicon substrate after the thermal treatments. The oxides showed excellent electrical properties in term of interface states and leakage currents.



(a) (b)

Fig. I.3.4: ***(a)*** *Oxide thickness on strained silicon films (grown on SiGe layers) as a function of the Ge content (and thus strain level), after N_2 implantation ($10^{15}cm^{-2}$, 3KeV) and oxidation at 850°C,* ***(b)*** *Density of interface traps vs energy gap for various strain levels.*

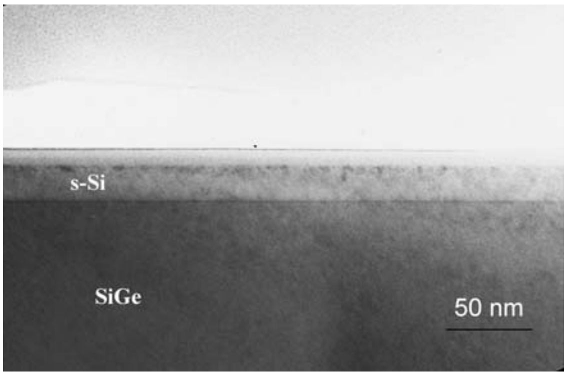


Fig. I.3.5: *TEM image of strained silicon overlayer after N_2 implantation and oxidation. We observe the full absence of extended defects.*

Task 3 Dopant diffusion in Germanium

3.a Implantation and diffusion of phosphorous in germanium

A. Chroneos, D. Skarlatos and C. Tsamis

The knowledge of the equilibrium diffusion behaviour of dopants is the basis for understanding diffusion mechanisms at the microscopic level. In contrast to silicon, research on diffusion of dopants in germanium has been initiated only in the last years, both for n-type and p-type dopants. In this work we investigate the diffusion of ion implanted phosphorous in germanium. The germanium wafers were implanted with 30 keV, 50 keV and 150 keV phosphorous ions at a various doses ranging from 10^{13} cm^{-2} to 10^{15} cm^{-2}. The samples were furnace annealed in inert ambient (N_2) at a wide range of temperatures (500-700°C) and times. The annealing conditions were chosen properly in order to avoid transient enhanced diffusion phenomena. The experimental concentration profiles, obtained by SIMS, were simulated using Synopsys-Taurus in order determine the diffusion coefficient of phosphorous in Ge under intrinsic and extrinsic diffusion conditions. In the case of uncovered samples substrate evaporation and phosphorous dose loss was observed, even at 500°C (fig. I.3.6).

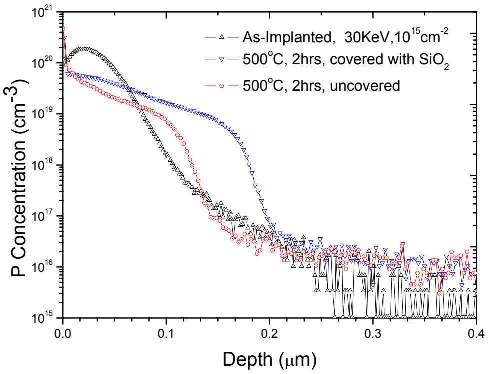


Fig. I.3.6: *SIMS profiles of P after implantation at 30KeV with a dose $10^{15}cm^{-2}$ and after annealing at 500 °C for 2hrs. For the uncovered samples substrate evaporation and phosphorous dose loss was observed.*

3.b Atomic scale simulations of the As-vacancy complexes in germanium

A. Chroneos, R. W. Grimes[*] and C. Tsamis,

Atomistic simulation has been used to study vacancy-assisted arsenic diffusion in germanium. The structures and relative energies of a series of different arsenic-vacancy complexes in germanium were considered (fig. I.3.7). In all cases the calculations used a plane-wave basis set and pseudo-potentials within the generalized gradient approximation (GGA) of the density functional theory (DFT). Plane-wave pseudo-potential DFT is a reliable theoretical technique in the field of point defects in semiconductors. The present work reproduces experimental and theoretical results for the formation energies of a range of point defects and defect complexes in Si. Additionally, the calculations for Ge highlight the important differences in the formation and binding energies of several arsenic-vacancy and related complexes in germanium compared to Si. In both host materials the nature of binding between defects can be understood in terms of the release of elastic energy around the defects (arsenic substitutional species and vacancies) and the changes in chemical bond configurations (dangling bonds).

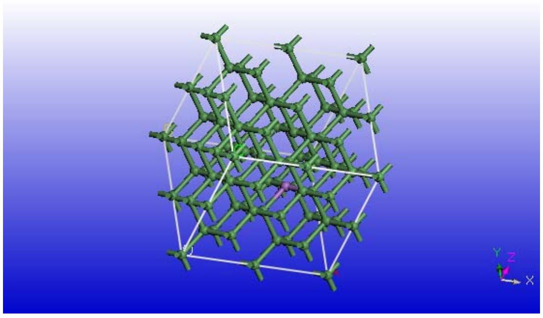


Fig. I.3.7: *A supercell of 62 germanium atoms and an arsenic-vacancy complex.*

****This work is performed in collaboration with the Department of Materials, Imperial College London, SW7 2BP,UK***

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. “Interstitial injection in silicon after high dose low energy arsenic implantation and annealing”, C. Tsamis, D. Skarlatos, V. Valamontes, G. BenAssayag, A. Claverie and W. Lerch, Applied Physics Letters 87,201903 (2005)
2. “Oxidation Enhanced Diffusion of boron in very low energy N_2^+ - implanted Silicon”, D. Skarlatos, C. Tsamis, M. Perego and M. Fanciulli, Journal of Applied Physics 97(1) (2005)
3. “Interstitial injection during oxidation of very - low energy nitrogen implanted – Silicon”, D. Skarlatos, C. Tsamis, M. Perego, M. Fanciulli and D. Tsoukalas, Materials Science and Engineering B 124-125, p. 314-318 (2005)
4. “Injection of point defects during annealing of low energy arsenic – implanted Silicon”, C. Tsamis, D. Skarlatos, V. Valamontes, G. BenAssayag, A. Claverie and W. Lerch, Materials Science and Engineering B 124-125, p. 261-265 (2005)

CONFERENCE PRESENTATIONS

1. “Interstitial injection during oxidation of very - low energy nitrogen implanted – Silicon”, D. Skarlatos , C. Tsamis , M. Perego, M. Fanciulli and D. Tsoukalas, E - MRS 2005 Spring Meeting , 31 May – 3 June, Strasbourg, France (Poster)
2. “Injection of point defects during annealing of low energy arsenic – implanted Silicon”, C. Tsamis, D. Skarlatos, V. Valamontes, G. BenAssayag, A. Claverie and W. Lerch, E - MRS 2005 Spring Meeting, 31 May – 3 June, Strasbourg, France (Poster)
3. “Boron Diffusion during thermal oxidation of very low energy nitrogen implanted silicon”, D. Skarlatos, C. Tsamis, M. Perego, M. Fanciulli, XXI Panhellenic Solid State Physics Conference, Nicosia, Cyprus, 28 - 31 August 2005 (Poster)

M.Sc. THESES

1. “Study of the recombination velocity of silicon interstitials at inert SiO_2/Si interfaces”, P. Tsouroutas, Msc. Degree in “Microsystems and Nanodevices”, National Technical University of Athens / NCSR “Demokritos”, October 2005, Supervisor: D. Skarlatos

Project: I. 4: THIN FILMS by CHEMICAL VAPOR DEPOSITION (CVD)

Project leader: Dr D. Davazoglou
Post-doctorals: Dr V. Vamvakas
PhD students: G. Papadimitropoulos
Undergraduate students: G. Aspiotis, C. Favre
Collaborating scientists: Dr. D. Kouvatsos, Dr. M. Vasilopoulou

Funding:

- EU STREP IST PROTEAS PV System, Contract N^o ENK6-CT-2002-00674, 1/1/2003-31/12/2005

Objectives:

The objectives of this group include research and development in the following:
a) Process and material development
b) Characterization of CVD films
c) Applications

Main results in 2005

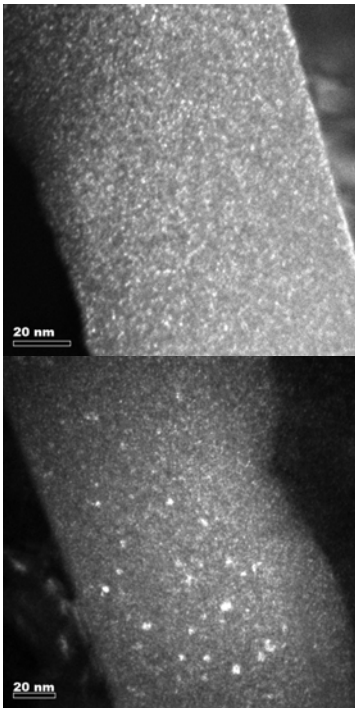
The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Characterization of Si rich Silicon nitride films prepared by LPCVD

V. Vamvakas

Si rich silicon nitride films were deposited by chemical vapor deposition at low pressures (LPCVD) from SiH_2Cl_2 (DCS) and NH_3 gas mixtures. Films stoichiometry was controlled by the DCS/NH_3 flow ratio.

The as deposited films were found to be homogeneous by transmission electron microscopy (TEM) measurements. After annealing at 950 °C Si nano-crystals (Si nc) were observed with size ranging between 1,0 and 1,5 nm (fig. I.4.1). Annealed at 1100 °C for 1h induced the formation of Si nc with dimensions of 4,5 to 5 nm (fig. I.4.1).



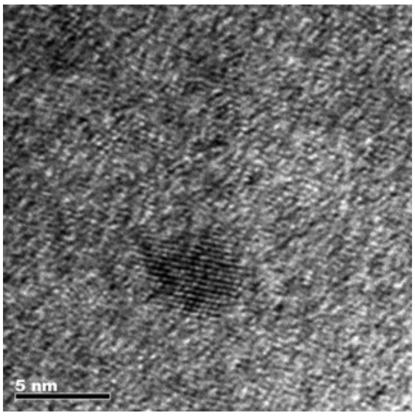


Fig. I.4.1: *TEM images of Si rich silicon nitride films prepared with a DCS/NH_3 ratio equal to 10 after annealing at 950 °C for 30 minutes (left top) and 1100 °C for 1h (left bottom). High resolution TEM image of a Si nc with size of 5,0 nm (upper).*

Fourier Transform Infrared Spectroscopy (FTIR) has shown that Si rich LPCVD silicon nitride films have a main transmission band near 830 cm $^{-1}$ corresponding to the stretching mode of vibration of the Si – N bond. As seen in fig. I.4.2, the increase of the Si content in films implies a slight shift towards higher wavenumbers of this absorption band.

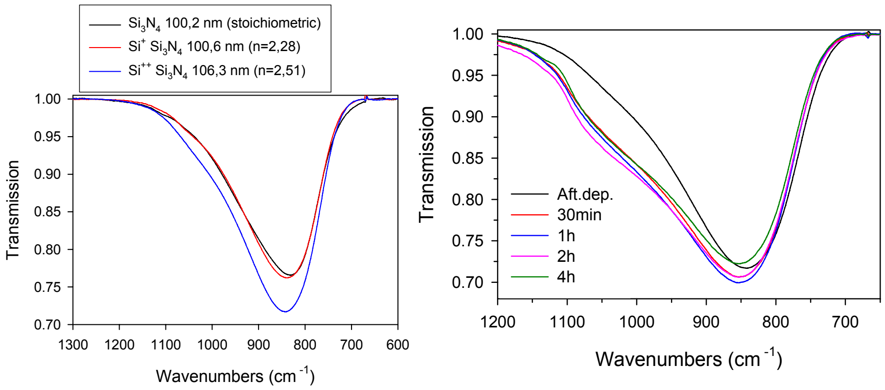


***Fig. I.4.2:**. (left) FTIR Transmission spectra of three Si-rich silicon nitride films with different Si content. (Right) FTIR spectra of Si rich silicon nitride films annealed at 1100 °C for several time periods.*

Annealing Si rich LPCVD silicon nitride films causes the appearance of an extra absorption band near 1075 cm $^{-1}$ (fig. I.4.2) probably connected to the presence of oxygen in films.

Task 2 Metal and metal oxide films

a. Metal-Organic Chemical Vapor Deposition (MOCVD) of Cu films – Selective deposition

G. Papadimitropoulos

A new MOCVD reactor for the deposition of Cu was installed (see figure). CupraSelect® vapors, which is the industry standard, are directly injected in the reactor in the liquid phase. The reactor operates within the temperature range 90 to 250 ^{o}C and pressures ranging between several mTorr to 10 Torr. The reactor is equipped with a hot filament for several purposes: 1) Heat the reactant gases during deposition and accelerate the growth rate and 2). W filaments when heated at high temperatures and at pressures of 10^{-2} Torr emit nano-particles of WO_x, which form films with a nano-columnar morphology (see fig. I.4.6). Morphology and composition of these films depend on the temperature of the filament during deposition. Such films may find applications as adhesion promoters for Cu deposition, templates for nano-particle deposition, nano-devices, gas sensors, etc. Other may be considered applications based on the combination of the two materials (Cu and WO_x) in the same reactor.

Fig. I.4.3: *MOCVD system developed in 2005. Left, a view of the MOCVD system. The electronics, the DLI system and the stainless steel reactor are shown. On the right, a photo of the interior of the reactor is shown. The ring-like injector, the W filament and the substrate are distinguished.*

Cu films were deposited by metal-organic chemical vapor deposition (MOCVD) using the installed MOCVD reactor with direct liquid injection (DLI) of CupraSelect® (hfacCu^{I}VTMS). Uniform films were obtained on 3 in. Si wafers covered with LPCVD W by pyrolysis of $W(CO)_6$ vapors, at temperatures ranging between 100 and 180 ^{o}C.

The roughness of Cu films was found to increase with temperature as shown by AFM measurements (see fig. I.4.4).

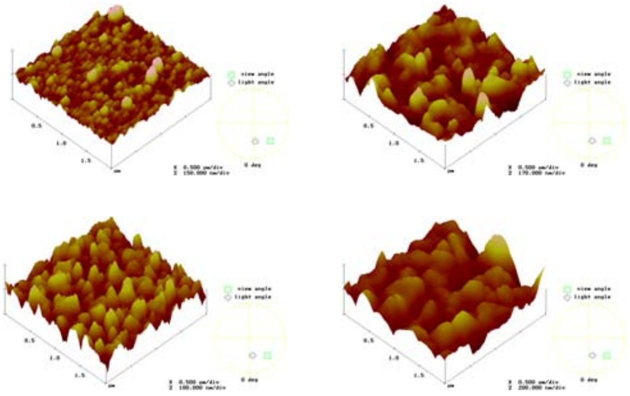


Fig. I.4.4: *AFM images taken on the surface of MOCVD Cu films deposited at 100 (upper left), 120 (upper right), 150 (lower left) and 180 ^{o}C (lower right).*

Under specific conditions selective deposition of Cu has been achieved on oxidized Si wafers covered by an LPCVD W layer and patterned with AZ5214 photoresist. Selective CVD has been performed on the entire surface of 3 in Si wafers.

b. Cu oxide films

G. Papadimitropoulos, N. Vourdas

Copper oxide films were grown by oxidation of vacuum evaporated copper layers on silicon substrates. Oxidation was made at atmospheric pressure, in a nitrogen-oxygen mixture 10% in oxygen and at temperatures varying between 185 and 450°C. X-rays diffraction (XRD) patterns showed that, dependent on oxidation temperature, films were entirely composed either of Cu_2O, at 225 °C, or of CuO above 350 °C and of mixtures of these oxides and Cu silicide at other temperatures. The optical properties of films were studied with spectroscopic ellipsometry measurements within the energy range 1 to 3,5 eV (see fig. I.4.5). The band gap, as defined by the Tauc model, was found equal to 2.3 eV for the Cu_2O and between 1,05 and 1,2 eV for CuO. It was shown that the gap of the Cu_2O films was free of localized states (see fig. I.4.5), which was not the case for the gap of CuO.

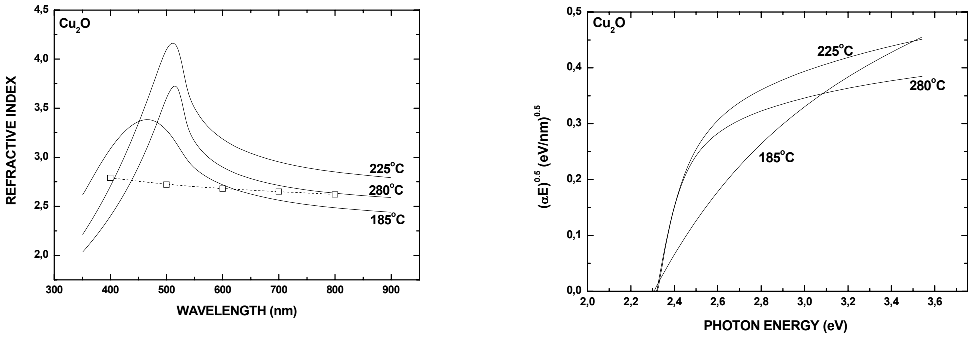


***Fig. I.4.5: (Left)** Dispersion of the real part of the refractive index of Cu_2O films grown at various temperatures. Data for single-crystalline material are also shown. **(Right)** Tauc' s plots for the above films.*

c. W oxide nano-structured films

G. Papadimitropoulos

Films composed of tungsten sub-oxides (WO_x, x<3) are deposited into the reactor used for Cu deposition by heating a W filament at a moderate vacuum of the order of 10^{-2} Torr. These films are composed of nano-rods with diameter of 10-40 nm, high porosity and are amorphous when currents between 25 and 35 A pass through the W filament. At higher currents they become crystalline. In fig. I.4.6 SEM and AFM micrographs taken on the surface of such a film are shown and the high film porosity is observed. These nano-structured films may find many applications such as barriers against Cu diffusion, nano-rod transistors, gas sensors, etc.

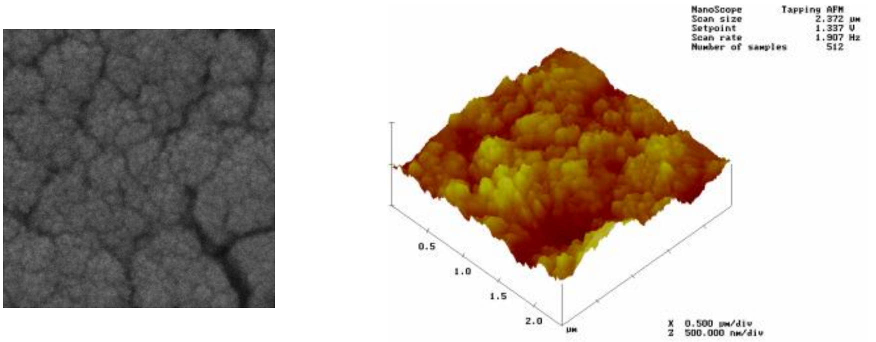


***Fig. I.4.6: (Left)** SEM micrograph taken on a $1x1 \mu m^2$ area on the surface of a nano-structured WO_x film. **(Right)** AFM micrograph taken on the surface of the same film.*

Task 3

a. *Gas sensors-Electrochromic Displays*

M. Vasilopoulou, D. Economou, C. Favre, G. Aspiotis

SnO_2 films were deposited on Si and glass substrates by atmospheric pressure chemical vapor deposition (APCVD) using a reactor entirely made of quartz and Teflon by oxidizing $SnCl_4$ vapors. Deposition was carried out at atmospheric pressure and at temperatures varying between 350 and 450 ^oC. The SnO_2 films were characterized by X-ray diffraction, FTIR spectroscopy, AFM and spectroscopic ellipsometry measurements.

Gas sensors were fabricated using SnO_2 films (see fig. I.4.7) and their electrical and sensing properties were tested in H_2. Reversible changes of electric conductance of films were observed when activated with Pt.

All solid-state electrochromic displays (see fig. I.4.7) were fabricated by tungsten oxide films on SnO_2:F covered glass substrates and using solid or gel-like organic electrolytes. These ionically conductive and electronically insulating electrolytes were based on poly (methyl methacrylate) (PMMA) and poly(2-hydroxyethyl methacrylate) (PHEMA) into which phospho-11 dodecatungstic acid ($H_3PW_{12}O_{40}$) was added at various concentrations. It was found that the degree of coloration does not depend on acid concentration.

Fig. I.4.7: *An all solid-state electrochromic display*

b. Packaging of concentration solar cells

V. Vamvakas

This activity focuses on the encapsulation of concentration solar cells used on PROTEAS, which is a hybrid solar system able to produce electric power, heat (hot water) and cooling power. In order to be economically viable, solar systems must have a long life (20 years or more) under extreme conditions. To insure the long life of the concentration solar cells used on PROTEAS a special encapsulation scheme, based on the use of poly-dimethyl siloxane (PDMS), was conceived (see fig. I.4.8).

Fig. I.4.8: (Left) *Photo of an encapsulated concentration solar cell. A prism ensuring the even distribution of energy on its surface and the current leads are integrated on the encapsulation.* ***(Right)*** *Photo of a cell ready to be positioned on PROTEAS.*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. “Influence of the annealing temperature on the IR properties of SiO_2 films grown from SiH_4+O_2”, V. Em. Vamvakas and D. Davazoglou, Miroelectronics Reliability, 45 (2005) 986–989
2. “Characterization of various insulators for possible use as low-k dielectrics deposited at temperatures below 200 °C”, M. Vasilopoulou, A. M. Douvas, D. Kouvatsos, P. Argitis and D. Davazoglou, Miroelectronics Reliability, 45 (2005) 990–993
3. “Influence of the growth temperature on the atomic distribution of TEOS deposited SiO_2 films”, V. Em. Vamvakas and D. Davazoglou, Journal of Vacuum Science and Technology B, Vol. 23, 1956 (2005)

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Simulation of FTIR spectra in non-normal incidence”, K. Zogopoulos, V. Vamvakas and D. Davazoglou, J. Phys.: Conf. Ser. Vol. 10. p. 194 (2005)
2. “Doping dependence of the adsorption of proteins on proton doped WO_3 films”, V. Asimakopoulos, C. Mastichiadis, S. Kakabakos and D. Davazoglou, J. Phys.: Conf. Ser. Vol. 10. p. 321 (2005)
3. “Fabrication of WO_3 –based electrochromic displays using solid or gel-like organic electrolytes”, M. Vassilopoulou, G. Aspiotis and D. Davazoglou, J. Phys.: Conf. Ser. Vol. 10. p. 329 (2005)
4. “Deposition and characterization of copper oxide thin films”, G. Papadimitropoulos, N. Vourdas, V. Em. Vamvakas and D. Davazoglou J. of Phys. Conf. Ser. Vol 10 (2005) 182-185.
5. “Calculation of the Infrared optical constants of LPCVD and thermally grown SiO2 films by measurements of reflection in non-normal incidence”, K. Zogopoulos, V. Vamvakas and D. Davazoglou, Electrochemical Society Proc. Vol. 2005-09, p. 291 (2005).
6. “Chemically vapor deposited SnO_2 films by oxidation of $SnCl_4$ vapors. Films characterization and application in gas sensors”, C. Favre, N. Vourdas, E. Pimienta V. Em. Vamvakas and D. Davazoglou, Electrochemical Society Proc. Vol. 2005-09, p. 952 (2005).
7. "Characterization of various low-k dielectrics for possible use in applications at temperatures below 160 C", M. Vasilopoulou, S. Tsevas, A.M. Douvas, P. Argitis, D. Davazoglou and D. Kouvatsos, Journal of Physics: Conference Series, 10, 218, October 2005.
8. “PROTEAS: a hybrid device for the production of electricity, heat and cooling power”, A. Papadopoulos, K. Chrysagis, S. Karvelas, D. Dousis, J. Lutz, Y. Spanoudakis, Y. Aspiotis, I. Luque-Heredia, J. M. Moreno, P. H. Magalhaes V. Emm. Vamvakas, M. Mathioulakis and D. Davazoglou, Proceedings of the 20th European Photovoltaic Solar Energy Conference, pp.2242-2245, Barcelona, 2005

CONFERENCE PARTICIPATION

1. “Chemically vapor deposited SnO_2 films by oxidation of $SnCl_4$ vapors. Films characterization and application in gas sensors”, C. Favre, N. Vourdas, E. Pimienta V. Em. Vamvakas and D. Davazoglou, 15th European Conference on Chemical Vapor Deposition (EUROCVD 15), Bochum, Germany, 5-9 Sept. 2005.

M.Sc. THESES

1. “Study of the adsoprion of proteins on tungsten oxide (WO_3) thin films”, V. Asimakopoulos
2. “Fabrication of an electrochromic display based on tungsten oxide thin films”, D. Oikonomou

DIPLOMA THESES

1. “Chemical vapor deposition of SnO_2 films. Application of these films in the fabrication of gas sensors.”, C. Favre

PROGRAM II
NANOSTRUCTURES and NANOELECTRONIC DEVICES

Programme representative: Dr N. Glezos

General

The overall research objectives of program II are as follows:

- To develop nanostructured and molecular materials with properties enabling their use in novel nanoelectronic and optoelectronic devices with emphasis on applications in information storage and processing
- To investigate both theoretically and experimentally the physics and technology of semiconductor nanostructures and molecular materials with emphasis on Si and Ge quantum dots and wires. Advanced electrical, optical and structural characterization methods are used to investigate transport, tunneling, charging and light emission mechanisms.
- To develop novel fabrication routes based on self-assembly techniques, advanced semiconductor processing and organic thin film deposition in order to fabricate useful nanostructures, such as silicon nanocrystals and nanowires in dielectrics, and functional molecular materials for nanoelectronic applications
- To fabricate nanostructure- and molecular-based electronic and optoelectronic devices (e.g. nanocrystal memories, organic FETs, light emitting devices) and to investigate their properties
- To evaluate the performance of the produced devices and assess the manufacturability of the developed technologies in an industrial environment.

IMEL has been involved in research and development of silicon nanostructures and the corresponding devices compatible with CMOS technology from the early nineties. Thanks to its accumulated know-how, its facilities and infrastructure, and its international partnership, IMEL keeps a pole position in the field of Si nanostructures and nanoelectronics at EU and at international level. The operating structure of IMEL offers the flexibility necessary for making the cross-point between Academia and industrial R & D Centres. Finally, IMEL benefits from a strong cross-link with other research Institutes of NCSR Demokritos (Materials Science, Chemistry), providing the interdisciplinary network and partnership required for any prospect in nanoelectronics and molecular electronics.

Project II. 1: NANOSTRUCTURES FOR NANOELECTRONICS AND PHOTONICS

Project leader: Dr A. G. Nassiopoulou

Key researchers: Dr A. G. Nassiopoulou, Dr N. Papanikolaou and Dr S. Gardelis

Phd students: M. Kokonou, A. Olziersky, A. Salonidou, A. Zoy

Main external collaborators in 2005: Dr A. Travlos and Dr K. Giannakopoulos (IMS-NCSR Demokritos), Dr I. Berbezier and A. Karmous (L2MP-CNRS France), Dr T. Stoica (ISGI-Juelich-Germany), Prof. A. Nazarov (Kiev)

Funding:

- EU IST NoE SINANO, 1/1/2004-31/12/2006, Contract N^{o}: 506844
- EU IST NoE MINA-EAST, 1/5/2004-30/4/2006, Contract N^{o}: 510470

Research orientation:

- Fabrication and characterization of semiconductor nanostructures (quantum wires, quantum dots, optical properties, charging effects, self-assembling, ordering) and theirs applications in non-volatile memories and photonic devices
- Fabrication and characterization of anodic porous alumina on silicon and its use in nanofabrication
- Self-assembled building blocks for nanoelectronics (self-assembly of nanoparticles, application in nanoelectronic devices, transport properties)
- Thermal transport in nanostructures

The activity on semiconductor nanostructures started at IMEL at the early nineties, within the framework of the Esprit project EOLIS (1992-1996) (pioneering work at IMEL on silicon nanopillars) and continued within the EU projects IST FET SMILE, contract No 28741, IST FORUM FIB, contract No 29573, and continues at present within the EU projects IST NoE SINANO and IST NoE MINA-EAST. The focus is on quantum dots and wires and their use in emerging electronic (e.g. nanocrystal memories) and photonic devices.

The activity on self assembly started at IMEL within the EU project IST FET Escher, contract No 33 287. In general, the concept of self-assembly has become very popular the last years, because it offers a possible way for creating potentially useful structures of the size of few nanometers or tens of nanometers. Self-assembly is seen as a good candidate for a new fabrication technology for the future information processing devices. IMEL is involved in the investigation of Au nanoparticles self-assembled between electrodes by dielectrophoresis and their use in bio-sensing.

Another interesting activity concerns anodic porous alumina thin films on silicon. A lot of work has been devoted in the literature to anodic porous alumina on bulk aluminum. Free standing porous alumina membranes with very regular pores vertical to the surface are fabricated and used in diverse applications, as for example in nanoparticle filters. More recently, porous alumina thin films are fabricated on a silicon substrate by anodization of Al thin films. They are used either as templates for the growth of different nanostructures through the pores (nanowires, quantum dots), or as matrices for the fabrication of composite materials. Very thin alumina films were fabricated on silicon at IMEL, with very regular vertical pores, which are very appropriate for the development of different nanopatterning and self-assembly techniques.

Thermal transport in nanostructures is a theoretical activity with important impact on applications in sensors. It is carried out in collaboration with research scientists of programme III.

Main results in 2005

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 LPCVD growth of double-layers of silicon nanocrystals within the gate dielectric of a MOS structure for improved non-volatility in nanocrystal memories

A Salonidou and A. G. Nassiopoulou
In collaboration with K. Giannakopoulos and A. Travlos from the Institute of Materials Science for TEM work

Layers of silicon nanocrystals embedded in SiO_2 are fabricated in this work by low-pressure chemical vapor deposition (LPCVD) of amorphous Si, followed by high temperature oxidation. The thickness of the amorphous layer as well as the oxidation time is adjusted so as to get the desired thicknesses of the nanocrystal layer and the top oxide. This process shows the advantage of controllable nanocrystal size and a good quality barrier silicon oxide.

By using the above process, single and double layers of silicon nanocrystals were fabricated within the gate dielectric of a MOS memory structure. Double layers were found to improve substantially the retention characteristics of the memory.

Fig. II.1.1. shows TEM images of two samples (Z_2 (a) and L (b)) with double layers of Si nanocrystals. In sample L the two nanocrystal layers are close together, their inter-distance being equal to 1.5nm, and they are situated at a tunneling distance from the silicon substrate. The lower layer, close to the substrate, is composed of smaller dots (d=3nm) than those of the upper layer (d=5nm). In sample Z_2 the dot layers are composed of dots of equal diameter (d=3nm) and their inter-distance is much larger (13nm). In both cases, the retention characteristics of the structure are improved compared with a single dot layer structure. In the second case this improvement is significantly larger than in the first case; almost no charge loss was measured after 10^4s from writing time.

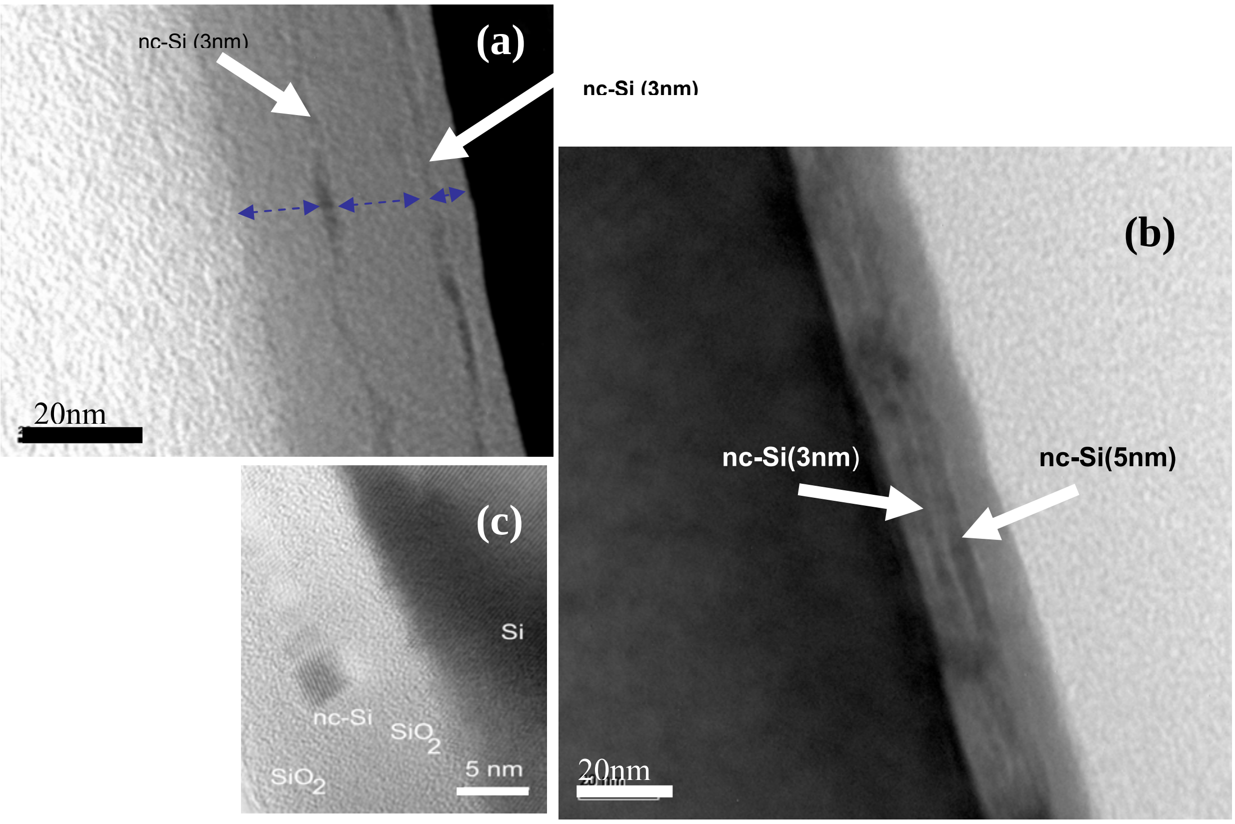
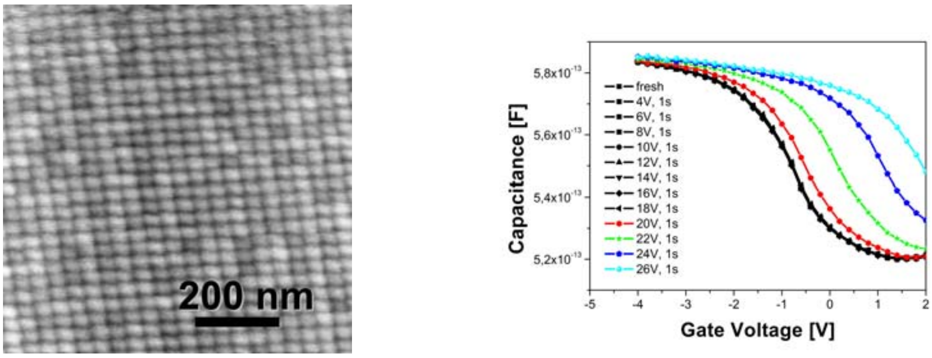


Fig. II.1.1: *Dark field TEM images of samples Z_2 and L with a double layer of silicon nanocrystals within SiO_2. In sample Z_2 (a) the gate stack is: SiO_2 (13nm)/Si-nc, d≈3nm/SiO_2-13nm/Si-nc, d≈3nm/SiO_2 (tunneling) 3,5nm/p-type Si substrate. In sample L (b) the gate stack is: SiO_2-8nm/ Si-nc, -d≈5nm/SiO_2-1,5nm/Si-nc, d≈3nm/SiO_2 - 3,5nm/p-type Si substrate. In (c) we see a high resolution dark field image of one nanocrystal of sample Z_2.*

Task 2 Ge dots in thin SiO_2 layers for application in non-volatile memories

A. Olzierski, E. Tsoi and A. G. Nassiopoulou

The use of Ge dots in a two-dimensional layer within SiO_2 as the charging medium in a MOSFET non volatile memory cell shows advantages compared with silicon nanocrystal NVMs. Due to the valence band offset between Ge dots and the Si substrate, better retention characteristics for holes compared with those achieved with silicon nanocrystals are expected. This approach is often described as dot storage engineering. Within this task, the growth of Ge nanocrystals in thin SiO_2 layers was studied and processes were developed, which include the fabrication of ordered and randomly distributed Ge dots in two-dimensional layers in SiO_2.



(a) **(b)**

Fig. II.1.2: (a) *AFM image of ordered Ge dots fabricated by FIB pre-patterning of the silicon surface, thermal oxidation to grow the tunnel oxide and dot growth by MBE.* ***(b)*** *Capacitance-Voltage characteristics of a capacitor using the ordered Ge dots within the gate dielectric.*

For the lateral ordering of the Ge dots, the combination of the following technological steps was used, in collaboration with $CRMC_2$ in France: a) use of a focused ion beam (FIB) to create ordered two-dimensional arrays of regular holes on a field oxide on the silicon substrate, b) chemical cleaning and restoring of the Si surface in the holes, c) further oxidation to transfer the pattern from the field oxide to the silicon substrate, d) removal of the field oxide and thermal re-oxidation of the sample in order to create a tunnel oxide of homogeneous thickness on the patterned silicon surface and c) self-assembly of the two-dimensional arrays of Ge dots on the patterned tunnel oxide. For the completion of the process and the fabrication of test structures (capacitors), a TEOS oxide was used as the control oxide (see fig II.1.2). Efficient charging of the structure by electron injection from the silicon substrate was demonstrated, resulting in a significant shift of the flat-band voltage of the MOS capacitor.

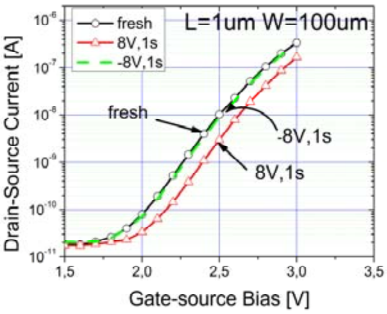


Fig. II.1.3: *I_{ds}-V_{gs} characteristic of the fabricated memory cell with non-ordered Ge dots.*

Randomly distributed Ge dot memory cells were also fabricated using e-gun evaporation of Ge on a tunnel SiO_2 layer, followed by TEOS deposition as the control oxide and rapid thermal annealing treatment at 1000°C for 250s. These cells demonstrate memory effect with a memory window of ~ 0.15 eV with write/erase voltages of +8 V, 1 s/-8 V, 1 s (see fig. II.1.3).

Task 3 Very thin anodic alumina templates on silicon for nanofabrication

M. Kokonou and A. G. Nassiopoulou

Porous anodic alumina is an extensively studied material due to its unique, self-organized structure that resembles a honeycomb. The last decade it has received additional attention due to its potential use as a masking or template material for the growth of nanowires and nanodots. For the fabrication of arrays of nanodots on silicon, it is highly desirable to reduce to the minimum the alumina template thickness, in order to facilitate dot growth through the pores and to have better and more accurate control on dot size and shape.

Within this task, anodic porous alumina films with thickness in the range of 20 to 50 nm were fabricated on a silicon substrate by electrochemistry, for use as templates for silicon nanopatterning and quantum dot growth. The anodization conditions were investigated in detail and it was found that they differ significantly from those used to grow thicker films. Much lower electric fields were necessary, since the strong electric field causes fast dissolution of the grown alumina. Anodization was done in sulfuric or oxalic acid aqueous solutions. Due to the low anodization voltage used, high density of pores was achieved. By using the optimum anodization conditions found, anodic porous alumina films on silicon with small diameter high density vertical pores homogeneously distributed in the film were fabricated and characterized by transmission electron microscopy.

Regular arrays of stoichiometric SiO_2 dots were grown on silicon through the pores of anodic porous alumina, during the same anodization process used for alumina formation. The SiO_2 dot diameter increases by increasing the anodization time and the dots merge together for excessively long times. By extensive characterization using AFM and TEM it was concluded that for short oxidation times after initiation of silicon oxidation a lower SiO_2 dot density is obtained (dot density is smaller than pore density), while many dots are at an inception stage. The height of the dots rapidly increases after nucleation, reaching values in the range of 8-10 nm. At long oxidation times dots continue to nucleate up to the pore density. The already nucleated dots increase in height and width, as resulted from AFM images, reaching saturation values at about 14 nm in height and 60 nm in width. From XPS and EELS spectra it was verified that the silicon oxide of the dots was stoichiometric SiO_2.

Fig. II.1.4 shows on the left the anodization current density versus time during anodization for alumina growth, with subsequent SiO_2 dot growth at the pore tips. The vertical dotted line shows the point where the Al is fully consumed and the oxidation of the silicon substrate starts at each pore tip. In (a) we see a plan view TEM image of the alumina film and in (b) and (c) we see respectively AFM and EELS images of the SiO_2 dots, after removal of the alumina film.

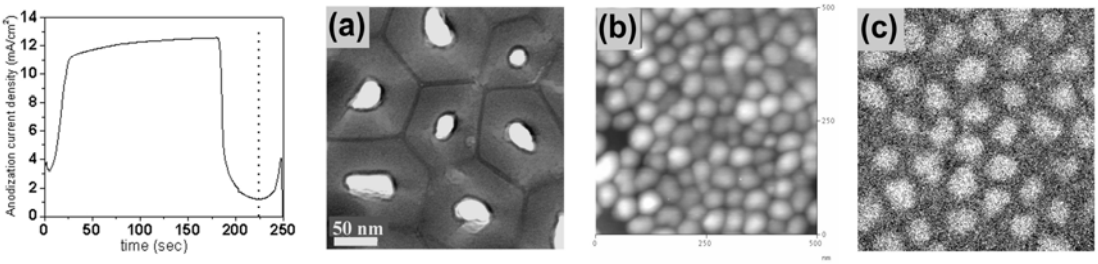
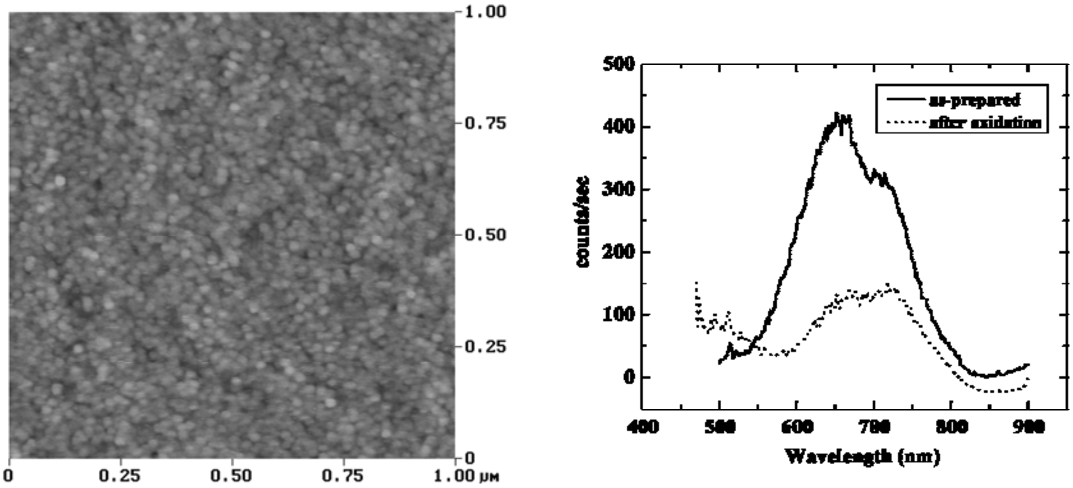


Fig. II.1.4: *The diagram on the left shows the anodization current density versus time. The vertical dotted line shows the point where the Al is fully consumed and the oxidation of the silicon substrate starts at each pore tip.* ***(a)*** *plan view TEM image of a nanoporous alumina film.* ***(b)*** *AFM image of arrays of SiO_2 nanoislands obtained by anodic oxidation through the pores of the alumina layer.* ***(c)*** *Oxygen mapping of the dots by electron energy loss spectroscopy (EELS) in a TEM.*

Task 4 Growth of silicon nanocrystals embedded in silicon dioxide for optoelectronic applications

S. Gardelis and A. G. Nassiopoulou

In this work we have grown silicon nanocrystals by anodization of bulk crystalline silicon in the transition regime using extremely short pulses (of few hundreds milliseconds duration) of anodic current in hydrofluoric acid- based solutions. This method produces a highly dense two-dimensional array of silicon nanocrystals isolated from each other as can be seen in the AFM image shown below (fig. II.1.5a). A typical size of these nanocrystals is 2.5-3 nm. Efficient photoluminescence was observed at room temperature peaked typically at 600-650 nm (fig. II.1.5b), originating from the silicon nanocrystals. After controlled oxidation of the layers in dry oxygen atmosphere at 850°C we managed to obtain silicon nanocrystals embedded in silicon dioxide, as the Fourier Transform Infra Red (FTIR) measurements demonstrate. The nanocrystals continue to emit in the red, however with reduced intensity compared to those in as-grown samples, whereas a second luminescence band peaked at 500 nm appears (fig.II.1.5b). This band shows a fast decrease in the intensity under laser illumination and originates from oxide-related defects. This growth method could be proved a cheap method to produce silicon nanocrystals for optoelectronic applications.



(a) (b)

Fig II.1.5: ***a)*** *AFM image of a two-dimensional array of silicon nanocrystals formed by anodization of crystalline silicon using extremely short pulses of anodic current.* ***b)*** *Photoluminescence spectrum before and after oxidation.*

Task 5 Thermal transport in nanostructures

N. Papanikolaou

Heat transport in nanostructures like quantum dot arrays, multilayers, and nanowires show new interesting properties that do not exist in the bulk materials. In semiconductors, heat is transferred mainly by lattice vibrations. We use atomistic classical molecular dynamics simulations to study the thermal conductivity of SiC nanowires with diameter of a few nanometers. The atomic interactions are modeled by the Tersoff potential which can give a reasonable description of the lattice dynamics of SiC. Thermal conductivity is calculated by the so called non-equilibrium method. Heat is added and removed in two different positions of the wire by rescaling the velocities of the atoms. The resulting temperature gradient is used to calculate the thermal conductivity using Fourier law. Thermal conductivity is greatly reduced compared to the bulk while heat transfer is influenced by the diameter as well as the termination of the nanowires.

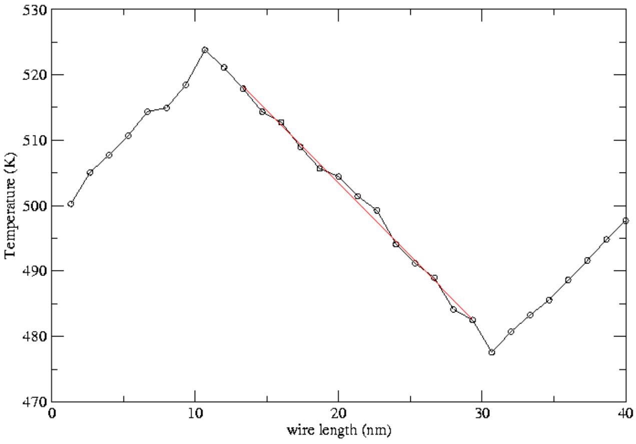


Fig. II.1.6: *Temperature gradient for a C terminated SiC wire of 4 nm diameter. Heat is added (removed) at around 10 (30) nm. The resulting profile is almost linear and it is an average over 800000 molecular dynamics steps.*

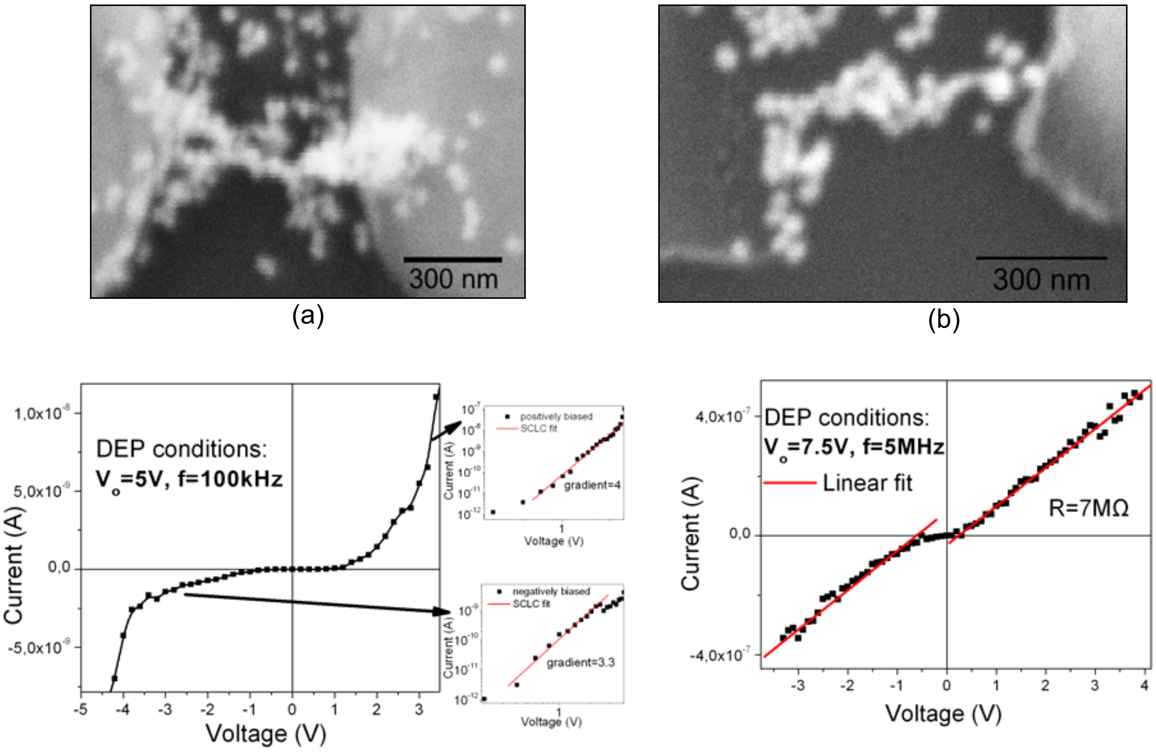
Phonon scattering at the wire surface is the main factor responsible for the reduction of the thermal conductivity. We plan to extend our study to include structural and chemical defects in the wires as well as study phonon scattering at interfaces of multilayer structures.

Task 6 Self assembly of gold nanoparticles by dielectrophoresis

A. Zoy and A.G. Nassiopoulou

In this work we develop the dielectrophoresis technique for controllable and rapid assembly of nanostructures between electrodes. This technique is based on the force exerted on the induced dipole moment of a dielectric or conductive particle by a non-uniform electric field. Alternative (AC) electric fields are often preferred in order to suppress electrochemical reactions, as for example electrolysis at the electrodes surface and to overcome the limitation of strong surface particle charge. DEP is suitable for microfluidic applications and nanoassembly.

At IMEL, dielectrophoresis is used for the controllable assembly of gold nanoparticles between electrodes and the formation of conductive nanowires with micrometer length. Different aqueous colloidal gold nanoparticles with average diameter of 20, 30, 40 and 45 nm were assembled between gold or platinum electrodes with 1 μm distance placed on a 150 nm thick SiO_2 layer. The effect of the frequency and strength of the applied field on the particle accumulation process was investigated. Two typical results at low and higher frequency including SEM images and corresponding current-voltage characteristics are shown in fig.II.1.7.



(a) (b)

(c) (d)

***Fig. II.1.7:** Two examples of nanowires formed between triangular Pt electrodes, using an AC field with **(a)** amplitude 5 V and frequency 100 kHz, **(b)** amplitude 7.5 V and frequency 5 MHz and **(c)** and **(d)** example of current-voltage characteristics of these structures.*

At low frequencies, the Au nanoparticles are aggregating as shown in the SEM image of a sample deposited with 5V voltage amplitude at 100 kHz in fig. II.1.7a. The corresponding I-V characteristic (fig. II.1.7c) is polynomial, which is indicative of space charge limited conductivity of the structure. Both parts of the I-V curve are presented in log-log scale in the inserts. At higher frequencies, the Au nanoparticles are deposited in a discrete way as shown in fig. II.1.7b (5 MHz). This sample exhibits a linear conductivity with the applied voltage in the range -3 to +3V, with a resistance of 7 MΩ, which is indicative of hopping transport between the Au nanoparticles.

PROJECT OUTPUT in 2005

PUBLICATIONS in REFEREED JOURNALS

1. “Structural study of very thin anodic alumina films on silicon by anodization in citric acid aqueous solution”, M. Kokonou, A. G. Nassiopoulou, K. G. Giannakopoulos, N. Boukos, A. Travlos, J.Nanoscience and Nanotechnology v.5, 1-5, 454-458, (2005)
2. “Ultra thin porous anodic alumina films with self-ordered cylindrical vertical pores on a p-type silicon substrate”, M. Kokonou, A. G. Nassiopoulou & K. P. Giannakopoulos, Nanotechnol. 16, 103, (2005)
3. "Optical properties of Si quantum wires and dots", X. Zianni and A. G. Nassiopoulou, Review Paper, Handbook of Theoretical and Computational Nanotechnology, edited by Michael Rieth and Wolfram Schommers, American Scientific Publishers, vol. 1 chapter 94, pages 1-37, (2005)
4. "Optical emission behavior of Si quantum dots", X. Zianni and A. G. Nassiopoulou, in "Quantum dots: Fundamentals, Applications and Frontiers" edited by: B. A. Joyce et al., NATO Science Series II. Mathematics, Physics and Chemistry, vol. 190, pages 369-376 (2005)
5. “Thin porous anodic alumina films: Interface trap density determination”, M. Theodoropoulou, P. K. Karahaliou, S. N. Georga, C. A. Krontiras, M. N. Pisanias, M. Kokonou, A. G. Nassiopoulou, IONICS, 11 (3-4): 236-239 2005

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Silicon nanocrystal memories by LPCVD of amorphous silicon, followed by solid phase crystallization and thermal oxidation”, E. Tsoi, P. Normand, A. G. Nassiopoulou, V. Ioannou-Sougleridis, A. Salonidou and K. Giannakopoulos, J. Phys.: Conf. Ser. 10 31-34 (2005)
2. “Charging characteristics of Si nanocrystals embedded within SiO_2 in the presence of near-interface oxide traps”, V. Ioannou-Sougleridis and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 39-42 (2005)
3. “Two-dimensional arrays of ordered, highly dense and ultra-small Ge nanocrystals on thin SiO_2 layers”, I. Berbezier, A. Karmous, A. Ronda, T. Stoica, L. Vescan, R. Geurt, A. Olzierski, E. Tsoi and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 73-76 (2005)
4. “Electrical conductivity of Au-nanoparticle-coated K_2SO_4 microcrystals deposited by DC trapping”, A. Zoy, A. G. Nassiopoulou, V. Ioannou-Sougleridis, M. Murugesan and B. D. Moore, J. Phys.: Conf. Ser. 10 105-108 (2005)
5. “Nanotemplate alumina films on a silicon substrate fabricated by electrochemistry”, M. Kokonou, A. G. Nassiopoulou, K. P. Giannakopoulos and N. Boukos, J. Phys.: Conf. Ser. 10 159-162 (2005)
6. “Interface traps density of anodic porous alumina films of different thicknesses on Si”, M. Theodoropoulou, P. K. Karahaliou, S. N. Georga, C. A. Krontiras, M. N. Pisanias, M. Kokonou and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 222-225 (2005)
7. “Ultrafast carrier dynamics in highly implanted and annealed polycrystalline silicon films”, E. Lioudakis, A. G. Nassiopoulou and A. Othonos, J. Phys.: Conf. Ser. 10 263-266 (2005)
8. “Semiconductor nanocrystals in thin SiO_2 layers for non-volatile memories”, A. G. Nassiopoulou, A. Salonidou, A. Olzierski, M. Kokonou, E. Tsoi, P. Normand, K. Giannakopoulos, Proceedings of the International workshop on semiconductor nanocrystals (SEMINANO) held in Budapest, September 10-12, 2005, p.p. 405-410 (2005)

PRESENTATIONS in CONFERENCES

1. “Self assembly of colloidal gold nanoparticles in-between micrometer electrode gaps by dielectrophoresis”, A. Zoy, A. G. Nassiopoulou, M. Murugesan andB. D. Moore, XXI Panhellenian Conference on Solid State physics and Materials Science, Nicosia, Cyprus 28-31 August 2005
2. “Arrays of SiO_2 nanoislands grown electrochemically on Si through nanoporous anodic alumina”, M. Kokonou, A. G. Nassiopoulou and K. P. Giannakopoulos, 3rd International Symposium on Nanomanufacturing (ISNM 2005), Nicosia, Cyprus, November 3-5, 2005

INVITED TALKS-LECTURES

1. “Silicon nanocrystals in thin SiO_2 layers for light emission and nonvolatile memories”, A. G. Nassiopoulou, (invited talk), First International Workshop on Semiconductor Nanocrystals (SEMINANO 2005), September 10-12, 2005, Budapest Hungary
2. “New challenges in nanoelectronics and sensors”, A. G. Nassiopoulou, (invited talk), WSEAS International Conference on Engineering Education, July 8-10, 2005, Athens, Greece
3. “From Micro to Nanoelectronics and Nanotechnology: Contribution to Society and National Economies”, A. G. Nassiopoulou (invited talk), Workshop on “Physics and the other Sciences”, Thessaloniki, 9 December 2005
4. "From Micro to Nanoelectronics and Nanotechnology: a revolutionary development", A. G. Nassiopoulou (invited talk, award of honorary plaque), Workshop on Micro and Nanoelectronics", TEI Lamias, 18 May 2005
5. “Nanotechnology at IMEL with applications in ICT, Health Care and Environment”, A. G. Nassiopoulou, Workshop: “NCSR Demokritos in a knowledge-based society”, Zappio, 6 July 2005

Project II.2: NANOCRYSTAL MEMORIES

Project leader: Dr P. Normand

Key Researchers: Dr P. Normand, Dr V. Ioannou-Sougleridis

Post-doctorals: Dr D. Skarlatos, Dr V. Vamvakas

PhD candidates: P. Dimitrakis, E. Kapetanakis, S. Kolliopoulou

Main External Collaborators in 2005: Prof. D. Tsoukalas (NTUA), Dr C. Bonafos and Dr G. BenAssayag (CEMES/CNRS), Dr B. Schmidt (FZR), Dr M. Petty (Univ. Durham), Dr A. Nylandsted (Univ. Aarhus)

Objectives:

- To develop novel high-throughput synthesis routes and techniques for creating nanoparticles in dielectrics, such as silicon nanocrystals in SiO_2 films by low-energy ion-beam-synthesis.
- To investigate the structural and electrical properties of the generated nanostructured materials and demonstrate material characteristics enabling the development of low-voltage high-density memory devices.
- To realize and evaluate nanostructure-based-memory devices and assess the manufacturability of the developed nanofabrication routes in an industrial environment.

Research orientation:

By associating the finite-size effects (e.g. Coulomb blockade) of nanocrystals and the benefits (robustness and fault-tolerance) of a stored charge distribution, the nanocrystal memories (NCMs) offer an attractive alternative for extending the scaling of conventional floating-gate memories (e.g. Flash EEPROMs). Our activities in this area started in 1996 through the development of the low-energy ion-beam-synthesis (LE-IBS) technique for producing nanocrystals in thin gate dielectrics. In collaboration with the University of Salford and the University of Thessalonique, generation of a 2D-array of Si nanocrystals in SiO_2 films by LE-IBS was demonstrated in 1997. This activity was further supported by the EU project, FASEM (1997-2000). LE-IBS Si-NCMs with endurance and write/erase times that approach those of DRAM were demonstrated in 1999. Observations of room-temperature single-electron storage effects in large-area n-channel Si-NC-MOSFETs were reported for the first time in 2002. Development of the LE-IBS technique with target the realization of manufactory non-volatile NCMs, has been conducted within the framework of the EU project, NEON (2001-2004), in collaboration with the US implanter manufacturer Axcelis.

In addition to our LE-IBS-NCM activities, major efforts have been devoted the last three years to the development of novel NCMs alternatives including, (a) Memory devices by Si^+ irradiation through poly-Si/SiO_2 gate stack in collaboration with Research Center Rossendorf and Zentrum Mikroelektronik Dresden, (b) Memory devices using Ge nanocrystals produced by molecular-beam epitaxy and rapid-thermal processing in collaboration with Aarhus University, (c) hybrid silicon-organic and SiGe-organic memories in collaboration with the University of Durham; this last activity was initiated within the framework of the EU IST-FET project, FRACTURE (2001-2003).

In 2005, the main focus in our activities was on the following four tasks:

1. Low-voltage Si nanocrystal memories obtained by low-energy ion-beam-synthesis
2. Channel edge effects in shallow-trench-isolated nanocrystal memories
3. Hybrid SiGe/organic MOSFET with self-assembled Au-nps for memory applications
4. Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride

Specific targets for 2006 include: (a) Fabrication of Si NCs of controlled size and interspacing by block-copolymer-assisted-nanopatterning in collaboration with project I.1, (b) development of a novel Si-NC synthesis route based on plasma-immersion ion-implantation in collaboration with CEMES/CNRS and one French SME (Ion Beam Services), (c) formation of oxide/nitride/oxide dielectric stacks with Si-NCs embedded in the nitride layer by LE-IBS and LPCVD for achieving fast memory devices with improved non-volatility.

Main results in 2005

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Low-voltage Si nanocrystal memories obtained low-energy ion-beam-synthesis

P. Dimitrakis, E. Kapetanakis, D. Tsoukalas, P. Normand

The realization of LE-IBS Si-nanocrystals into SiO_2-gate dielectrics for low-voltage non-volatile memory devices, is not trivial for two main reasons. First, the LE regime (typically around 1keV) does not allow the production of structures with asymmetrical oxide barriers such as the control oxide (CO) above the NC layer is thicker than the injection or tunnel oxide (TO). Second, the implantation doses required for NC fabrication severely damage the host matrix and efficient oxide healing using reasonable post-implantation annealing conditions remains a difficult task. A technical option to overcome these issues is based on post-implantation thermal treatments in nitrogen-diluted-oxygen ambient. Such an alternative results from a compromise between several requirements: (1) to keep a moderate thermal budget, (2) to form a high-density of separated and passivated NCs, (3) to enhance the insulating properties of the control oxide and obtain functional asymmetrical barriers. This can be achieved under slight oxidizing annealing conditions that should be carefully adjusted according with the implantation parameters.

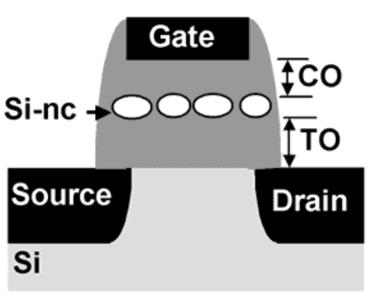


Fig. II.2.1: *A schematic cross-section of a nanocrystal memory device.*

In this direction, our 2005-activities have been concentrated first, on the thermal oxidation in N_2-diluted-O_2 of high-temperature pre-formed silicon NCs in collaboration with CEMES/CNRS (FR) and second, on the effect of the annealing duration and N_2/O_2 composition on the memory performance of Si-implanted-SiO_2 gate dielectrics. This last study is important not only to demonstrate that annealing in N_2/O_2 may provide a potential solution for generating functional LE-IBS NC gate dielectrics, but also to investigate if such an alternative can lead to a reliable process window. For this purpose, 7nm-thick SiO_2 oxides were implanted with 1keV Si ions to a dose of $2x10^{16}$ cm^{-2} and subsequently annealed at 950°C for 30 min in N_2/O_2 mixtures with oxygen contents ranging from 1 to 5%.

Typical memory windows obtained after application of 100ms symmetrical positive and negative gate pulses are presented in fig. II.2.2. For oxygen contents higher than 2%, the memory effect is dramatically reduced and almost disappears for the 5% O_2 regime. The attainable memory windows (~ 2V) are quite similar for the 1, 1.5 and 2% O_2 regimes while charge injection occurs at lowest voltages for the lowest O_2 content. This result is mainly attributed to injection oxide healing that reduces significantly the conductivity of the oxide and thereby, the trap-assisted-mechanism involved in NC charging. It should be noted here that any change in oxide conductivity affects the charge retention properties of the NC gate dielectrics and therefore, the best process window should result from a compromise between programming regime (voltage and speed) and retention time. Memory behavior of the above implanted oxides after annealing at 950°C in 1.5% O_2 for a duration ranging from 5 to 120min is reported in Tsoukalas et al., MSE B, 2005.

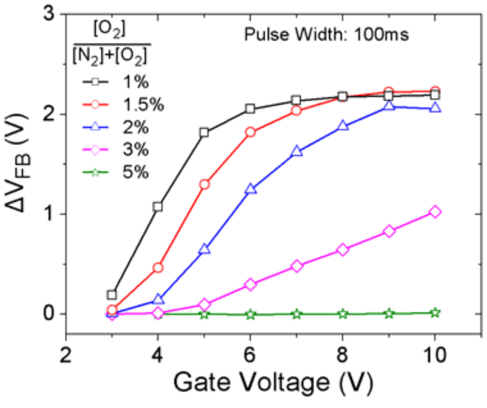


Fig. II.2.2: *Memory window characteristics obtained for MOS capacitors using 7nm-thick oxides implanted with 1keV Si to a dose of $2x10^{16}cm^{-2}$ and subsequently annealed in various oxidizing atmosphere.*

Task 2 Channel edge effects in shallow-trench-isolated nanocrystal memories

P. Dimitrakis and P. Normand

Within the framework of the EU project NEON, prototype LE-IBS-Si-nanocrystal memory devices were fabricated at STMicroelectronics (IT) on 8-inch wafers using a conventional process flow based on a 0.15μm Flash-EEPROM technology. The devices were isolated following a shallow-trench-isolation (STI) procedure. Capacitors and n-MOSFETs memory cells with gate lengths and widths ranging from 0.16 to 10 μm have been realized. Preliminary electrical investigations revealed that parasitic transistors (FET_P) formed at the channel edges affect drastically the device performance. The action of FET_P can be detected through a “subthreshold hump” in the transfer characteristics of the 10x10μm^2 and 0.9x0.6μm^2 (WxL) devices (see fig. II.2.3). Beyond this current hump, the device transcharacteristics correspond to that of the intrinsic transistor (FET_I) formed in the central part of the channel

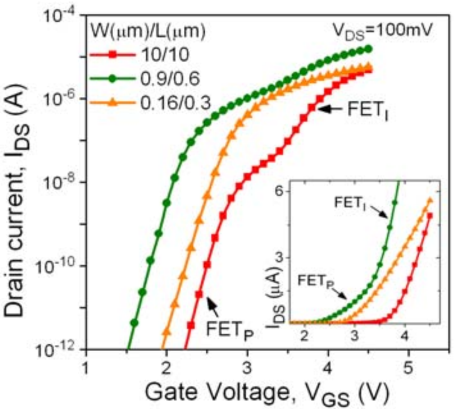


Fig. II.2.3: *Typical I_{DS}-V_{GS} curves of ULE-IBS-NCMs with different channel*

Major efforts have been devoted this year to understand and describe in a comprehensive way the effect of FET_P on the memory behavior of the devices. Memory testing revealed that the parasitic transistors can be programmed or erased but exhibit memory characteristics significantly different than that of FET_I. Typical results are shown in fig. II.2.4 where the memory windows are extracted from the transfer characteristics of the devices for different source-drain currents values. We also observed that the programming/erasing windows extracted from high I_{DS} in the case of 10μm/10μm devices are similar to the flat-band voltage shift curves obtained from large area (0.0096 cm^2) capacitors located on the same wafer than the transistors. This clearly indicates that any comparison in terms of memory behavior between capacitors and transistors will be misleading if the contribution of FET_P cannot be canceled. Finally, while no ‘subthreshold hump’ appears in the transfer characteristics of deep submicron (0.16x0.3μm^2) transistors, our investigations reveal that the parasitic transistors remain active and their operation dominates the memory behavior of the devices. The above findings stress out that the channel edge effects could constitute a technological issue towards the integration of nanocrystal floating-gate in conventional memory architecture.

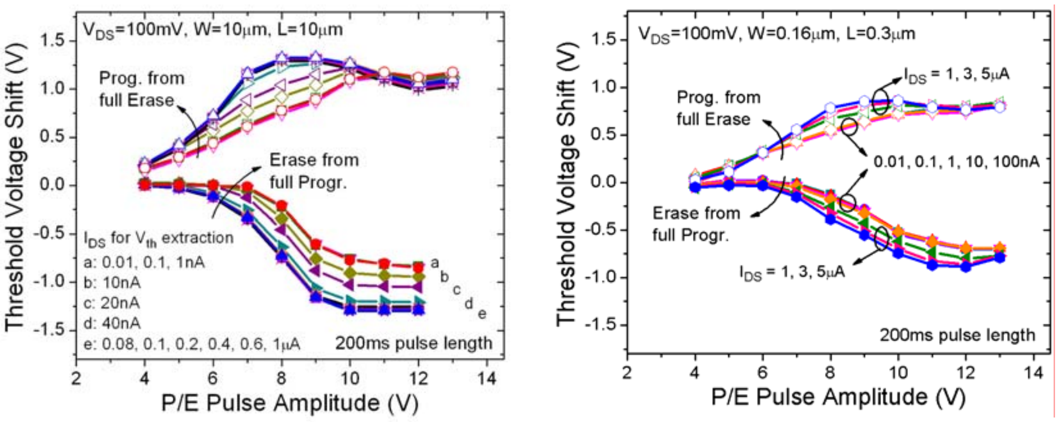


Fig. II.2.4: *Threshold voltage shift (ΔV_{th}) as a function of programming (P) and erasing (E) pulses for transistors with different channel areas: (left) W=10μm/L=10μm, (right) W=0.16μm/L=0.3μm. The P and E single pulses were applied from full E (-10V/200ms) and P (+8V/200ms) conditions, respectively, such as determined for 10μm/10μm FET_I and capacitors. ΔV_{th} has been calculated for different V_{th}-extraction I_{DS} values.*

Task 3 Hybrid SiGe/organic MOSFET with self-assembled Au-nps for memory applications

S. Kolliopoulou, P. Dimitrakis, D. Goustouridis, S. Chatzandroulis, P. Normand, D. Tsoukalas

Towards the realization of ultra-dense integrated circuits various technological approaches are currently explored. Three-dimensional (3-D) integration by using different 'memory' layers on the top of a silicon wafer where logic circuits are fabricated using conventional IC processing has been recently demonstrated. In this direction, our recent efforts have been devoted to the fabrication at low temperature of SiGe channel MOSFETs that allows further 3-D integration of multiple layers with functional devices [Kolliopoulou et al., Microelec. Eng., 2005]. The device fabrication procedure combines a low-temperature wafer-bonding process and the V-groove technique for channel definition. The latter is attractive since it can potentially lead to very short channel device architectures.

This year we concentrated our activities on the realization of low-temperature processed floating-gate type memory that combines the above V-groove SiGe MOSFET technology with deposition of charge storage nodes consisting of self-assembled Au nanoparticles (nps) and Langmuir-Blodgett (LB) films of organic insulators. A schematic diagram of the devices is shown in fig. II.2.5. Such structures were processed at a temperature lower than 400ºC. The 35-nm thick low-temperature oxide (LTO) of the gate stack was functionalized by surfactants containing amine groups. Au-nps were prepared separately and covered by specific organic ligands. Following functionalization, the SiGe sample was dipped into the Au-nps solution leading to the formation of a layer containing a high-density of well-ordered self-assembled Au-nps. Finally, 20 layers of Cadmium Arachidate were LB deposited to insulate the nanoparticles, and the gate electrode was then fabricated by Al evaporation and patterning.

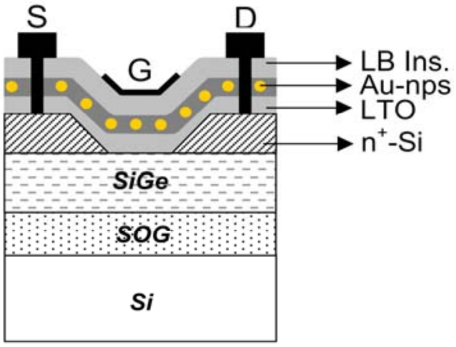


Fig. II.2.5: *A schematic cross-section of the hybrid organic-SiGe device with self-assembled Au-nps.*

The memory behavior of the devices was evaluated by applying positive and negative voltage pulses to the gate electrode while source and drain potentials were kept floating. For applied voltage pulses higher than ±12V, the threshold voltage of the devices is shifted with respect to the charges (electrons or holes) stored into (or extracted from) the nps. The I_{DS}-V_{GS} characteristics were monitored after gate pulsing in order to extract the threshold voltage. Such calculations were made according to the constant current method, and assuming a threshold drain-to-source current of 6.5×10^{-8}A. Memory windows as high as 7V for 1s programming time have been achieved (fig.II.2.6). It is important to note that due to the relatively thick LTO layer, the conduction properties of the LB insulator and the work functions of the used materials, electrons are extracted from the Au-nps to the gate electrode when applying positive gate pulses while pulses of opposite polarity cause electrons to move from the gate into the Au-nps.

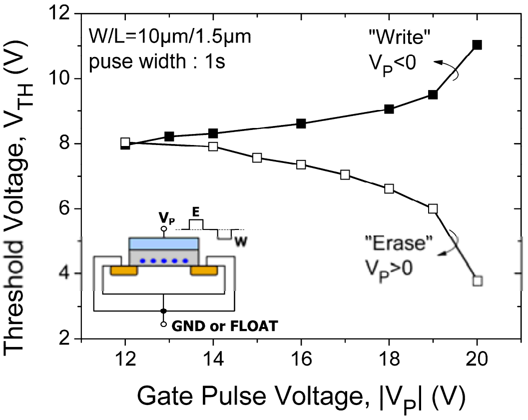


Fig. II.2.6: *Memory window characteristics of a hybrid organic/SiGe MOSFET with Au-nps.*

Task 4 Oxide/nitride/oxide dielectric stacks with Si nanocrystals embedded in nitride

V. Ioannou-Sougleridis, V. Vamvakas, P. Dimitrakis, D. Skarlatos, P. Normand

The use of thin tunnel SiO_2 layer (~2-3nm) in NCM technology allows high-speed operation at low voltages but addresses a critical issue for long retention times. If a thick oxide is used to enhance data retention, the advantage of high endurance and high speed at reasonable voltages is lost rapidly. Different alternatives have been suggested for improving the performance of NCMs operating in the direct tunneling regime. An interesting direction would be to combine the potential advantages (low-voltage and high-speed operation) of NCM technology with the advantages (long retention times, immunity to disturbance) of time-proven nitride-trap technology. Memory structures using SiO_2-Si_3N_4-SiO_2 (ONO) gate dielectric with nanocrystals embedded in the nitride layer are expected to gather together these advantages. While such an alternative, proposed by Motorola in 2002, has attracted a great deal of interest, much research and development is still required to establish a technology route that will be able to build a foothold in the NVM market.

In this direction, part of our research activities has been concentrated to the realization of Si-NC ONO structures where the Si-NCs are generated in the nitride layer by low-energy ion-beam-synthesis. SiO_2-Si_3N_4 structures were developed onto Si substrates and subsequently implanted at CEMES/CNRS with 1keV Si ions to a dose ranging from $5x10^{15}$ to $1.5x10^{16}$ cm^{-2}. The thickness of the oxide and nitride layers was 2.5nm and 6.5nm, respectively. After the steps of post-implantation annealing and SiO_2 deposition, gate electrodes were fabricated on part of the samples by Al evaporation and patterning. TEM examination of the 1keV /$1.5x10^{16}$ Si cm^{-2} implanted sample revealed the presence of Si-NCs into the nitride layer (see fig. II.2.7) together with a significant swelling of the SiO_2 and Si_3N_4 layers, respectively, 3.4 and 8.3nm in thickness. Preliminary investigations of the memory behavior of the above samples indicate enhanced charge storage (both electrons and holes) for the Si-NC ONO structures compared to the reference ONO samples (see fig. II.2.8). Typical memory windows attainable under pulse operation are shown in fig. II.2.9. In addition to our LE-IBS experiments, formation of Si-NC ONO structures by LPCVD of thin Si-rich-silicon nitride films and subsequent thermal annealing is currently examined in collaboration with project I.4.

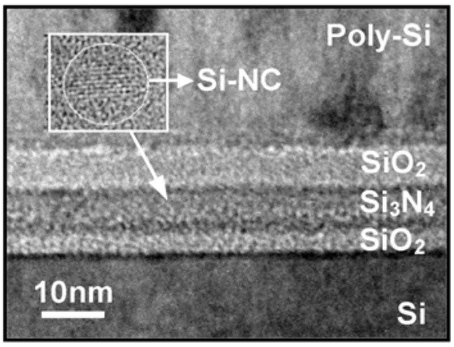


Fig. II.2.7: *Cross-sectional TEM picture of a Si-NC ONO structure. The NCs were generated in the nitride layer by LE-IBS (1keV / $1.5x10^{16}$ cm^{-2}).*

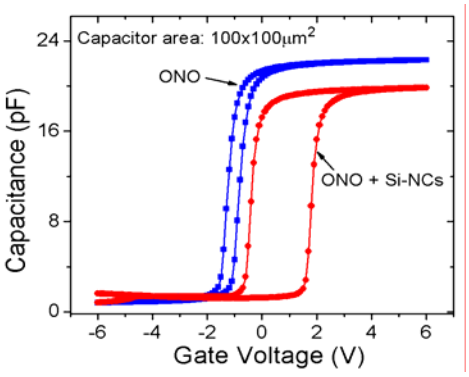


Fig. II.2.8: *Capacitance vs gate voltage round sweeps for ONO and Si-NC ONO dielectrics. The NCs were generated by LE-IBS (1keV / $1.5x10^{16}$ cm^{-2}).*

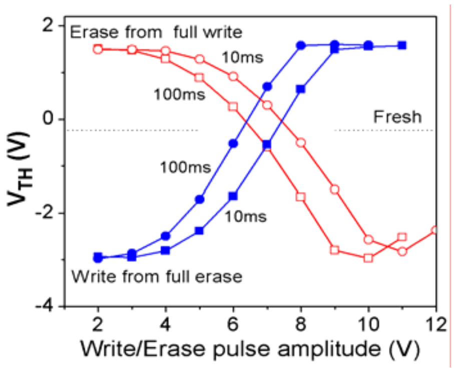


Fig. II.2.9: *Flat-band shifts after application of gate voltage pulses for Si-NC ONO dielectrics. The NCs were generated by LE-IBS (1keV / $1x10^{16}$ cm^{-2}).*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. "A Si/SiGe MOSFET utilizing low-temperature wafer bonding", S. Koliopoulou, P. Dimitrakis, D. Goustouridis, S. Chatzandroulis, P. Normand, D. Tsoukalas, H. Radamson, Microelectronic Engineering 78-79, 244 (2005).
2. "Recent advances in nanoparticle memories", D. Tsoukalas, P. Dimitrakis, S. Kolliopoulou, P. Normand, Mater. Sc. Eng. B 124-125, 93 (2005).
3. "Si nanocrystals by ultra-low energy ion implantation for non volatile memory applications", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, M. Carrada, G. Ben Assayag, A. Claverie, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, Mater. Sc. Eng. B 124-125, 499 (2005).
4. "Fabrication of nanocrystal memories by ultra low energy ion implantation", N. Cherkashin, C. Bonafos, H. Coffin, M. Carrada, S. Schamm, G. Ben Assayag, D. Chassaing, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, T. Muller, K. H. Heinig, A. Claverie, physica status solidi (c) 2,1907 (2005).
5. "Size and aerial density distributions of Ge nanocrystals in a SiO_2 layer produced by molecular beam epitaxy and rapid thermal processing", A. Kanjilal, J.L. Hansen, P. Gaiduk, A.N. Larsen, P. Normand, P. Dimitrakis, D. Tsoukalas, N. Cherkashin, A. Claverie, Appl. Phys. A 81, 363 (2005).
6. "Si nanocrystals by ultra-low-energy ion beam-synthesis for nonvolatile memory applications", C. Bonafos, H. Coffin, S. Schamm, N. Cherkashin, G. Ben Assayag, P. Dimitrakis, P. Normand, M. Carrada, V. Paillard, A. Claverie, Solid-State Electronics 49, 1734 (2005).

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1. "Semiconductor nanocrystal floating-gate memory", P. Dimitrakis and P. Normand, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D5.1, pp. 203-216, 2005.
2. "Manipulation of 2D arrays of Si nanocrystals by ultra-low-energy ion beam-synthesis for nonvolatile memories applications", C. Bonafos, N. Cherkashin, M. Carrada, H. Coffin, G. Ben Assayag, S. Schamm, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, T. Muller, K.H. Heinig, A. Argawal, A. Claverie, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D5.2, pp. 217-222, 2005.
3. "Ge nanocrystals in MOS-memory structures produced by molecular-beam epitaxy and rapid-thermal processing", A. Nylandsted Larsen, A. Kanjilal, J. Lundsgaard Hansen, P. Gaiduk, P. Normand, P. Dimitrakis, D. Tsoukalas, N. Cherkashin, A. Claverie, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D6.2, pp. 263-267, 2005.
4. "Oxidation of Si nanocrystals fabricated by ultra-low energy ion implantation in thin SiO_2 layers", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, M. Respaud, G. Ben Assayag, P. Dimitrakis, P. Normand, M. Tencé, C. Colliex, A. Claverie, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D6.6, pp. 281-286, 2005.
5. "Gold Langmuir-Blodgett deposited nanoparticles for non-volatile memories", S. Kolliopoulou, D. Tsoukalas, P. Dimitrakis, P. Normand, S. Paul, C. Pearson, A. Molloy, M.C. Petty, in Materials and Processes for Nonvolatile Memories*,* edited by A. Claverie, D. Tsoukalas, T-J. King, and J.M. Slaughter, Mater. Res. Soc. Symp. Proc. 830**,** Warrendale, PA, D6.7, pp. 287-292, 2005.
6. "Memory devices obtained by Si+ irradiation through poly-Si/SiO2 gate stack", P. Dimitrakis, P. Normand, E. Vontitseva, K.H. Stegemann, K.h. Heinig, and B. Schmidt, , in A. G. Nassiopoulou, N. Papanikolaou and C. Tsamis (Eds), Second Conference on Microelectronics, Microsystems and Nanotechnology, MMN-2004, Journal of Physics: Conference Series 10, pp. 7-10, 2005.
7. "Silicon nanocrystal memories by LPCVD of amorphous silicon, followed by solid phase crystallization and thermal oxidation", E Tsoi, P Normand, A G Nassiopoulou, V Ioannou-Sougleridis, A Salonidou and K Giannakopoulos, in A. G. Nassiopoulou, N. Papanikolaou and C. Tsamis (Eds), Second Conference on Microelectronics, Microsystems and Nanotechnology, MMN-2004, Journal of Physics: Conference Series 10, pp. 31-35, 2005.
8. "Field effect devices with metal nanoparticles integrated by Langmuir–Blodgett technique for non-volatile memory applications", S Kolliopoulou, D Tsoukalas, P Dimitrakis, P Normand, S Paul, C Pearson, A Molloy and M C Petty, in A. G. Nassiopoulou, N. Papanikolaou and C. Tsamis (Eds), Second Conference on Microelectronics, Microsystems and Nanotechnology, MMN-2004, Journal of Physics: Conference Series 10, pp. 57-60, 2005.

CONFERENCE PRESENTATIONS

1. "Control of Si nanocrystals fabricated by ultr-low energy ion implantation for non volatile memories", H. Coffin, C. Bonafos, S. Schamm, N. Cherkashin, M. Carrada, G. Ben Assayag, A. Claverie, P. Dimitrakis, P. Normand, M. Perego, M. Fanciulli, E-MRS 2005 Spring Meeting, Symposium D, Strasbourg, France, May 31 – June 3, 2005.
2. "Si nanocrystals by ultra-low-energy ion beam-synthesis for nonvolatile memory applications", C. Bonafos, H. Coffin, S. Schamm, M. Carrada, N. Cherkashin, G.B. Assayag, P. Dimittrakis, P. Normand, M. Perego, M. Fanciulli, Claverie, 1st International Conference on Memory Technology and Design (ICMTD), Giens, France, May 21-24, 2005.
3. "Metal nano-floating gate memory devices fabricated at low temperature", S. Koliopoulou, P. Dimitrakis, D. Goustouridis, P. Normand, C. Pearson, MC Petty, H. Radamson, D. Tsoukalas, International Conference on Micro- and Nano-Engineering, MNE 2005, Vienna, Austria, September 19-22, 2005. Best poster award – third price.

Ph. D. THESES

1. "Formation of semiconductor nanocrystals by ultra-low-energy ion-beam-synthesis and memory devices", E. Kapetanakis, National Technical University of Athens, April 2005, Supervisor: P. Normand
2. "Silicon nanoelectronic devices", S. Kolliopoulou, Aristotle University of Thessalonique, December 2005, Supervisor: D. Tsoukalas

INVITED TALKS

1. "Recent advances in nanoparticle memories", D. Tsoukalas, P. Dimitrakis, S. Kolliopoulou, P. Normand, E-MRS 2005 Spring Meeting, Symposium D, Strasbourg, France, May 31 – June 3, 2005.
2. "Nanocrystals and their application in nonvolatile memories", D. Tsoukalas, P. Dimitrakis, P. Normand, First International Workshop on Semiconductor Nanocrystals, SEMINANO 2005, Budapest, September 10-12, 2005.

Project II.3: MOLECULAR MATERIALS AS COMPONENTS OF ELECTRONIC DEVICES

Project leader: Dr N. Glezos

Key researchers: Dr N. Glezos, Dr N. Papanikolaou, Dr P. Argitis, Dr V. Ioannou-Sougleridis

Post Doctorals: Dr A.Douvas

PhD candidates: D.Velessiotis, G. Chaidogiannos, G.Tatakis

External Collaborators: Dr D. Yannakopoulou and Dr E. Mavridi (Institute of Physical Chemistry, NCSR "D"), Prof. S. Kennou (Department of Chemical Engineering, University of Patras), Dr S.Nespurek (Intitute of Macromolecular Science, Prague), Dr G.Papavasiliou (National Hellenic Research Foundation), Dr G. Kaltsas (Technical University of Athens)

Funding:

- EU RTN-STREP- project Uninanocups, 1/1/2004-31/12/2007, Contract N^o MRTN-CT-2003-504233
- NMP STREP TASNANO, 1/1/2005-31/12/2007, Contract N^o 516865
- GSRT bilateral project Greek – Czech, 29/7/2003-28/7/2005

Research orientation:

- To investigate the potential of molecular materials to be used as active components in molecular devices e.g. as switching or memory elements.
- To evaluate elements of the class of organic crystals as components of organic FETs
- To develop techniques for thin film deposition and characterization of molecular materials.
- To use ab-initio electronic structure methods which are more appropriate to study semiconductor properties to be able to address different problems.
- To develop more semiempirical atomistic methods like tight-binding in order to describe optical properties.

Main results in 2005

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Organic/inorganic composite materials as components of nano-devices

N. Glezos, A. M. Douvas, P. Argitis , D. Velessiotis and V. Ioannou-Sougleridis

A wide variety of organic molecules or metal nanoclusters have been proposed for molecular electronics applications in the past. Polyoxometalates (POMs) are inorganic metal-oxygen clusters that combine both the electron transport properties of the organic molecules with the charge confinement properties of the inorganic nanoclusters. POMs, especially the tungsten and molybdenum ones, have well-defined and stable structure consisted of clusters of coordination polyhedra MO_n that have a metal ion in their center and connect each other through common edges and apices. In previous work of our group, tungsten POMs were embedded into polymeric matrices using nano-distant planar electrodes, and conductivity peaks were evident even at room temperature conditions. During this year, the electric transport and charging properties of molecular monolayers consisted of POM anions and 1,12-diaminododecane (DD) cations, prepared with the layer-by-layer (LBL) self-assembly method were studied. It is shown that POM molecules act as electron traps and that tunneling dominates other transport mechanisms.

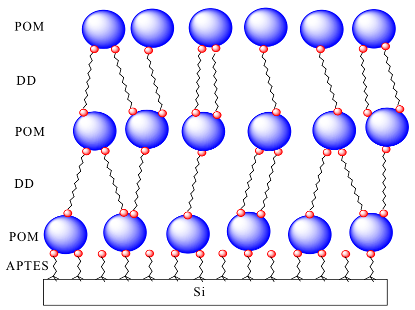


***Fig. II.3.1:** Schematic diagram of APTES-(POM-DD)$_2$POM multilayer film (3-POM-layer film) prepared with LBL method on Si wafer.*

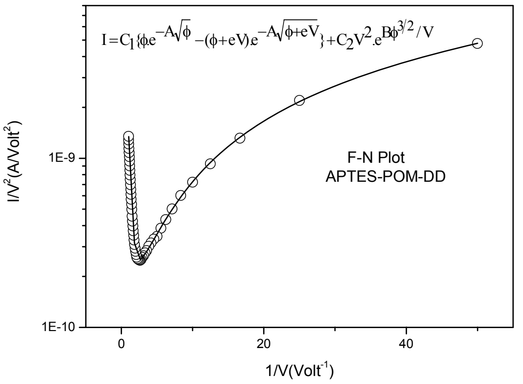


***Fig. II.3.2:** Comparison of experimental results (symbols) with tunneling theory (solid line). This method allows the determination of the average film thickness and the potential step due to the film added on silicon.*

Multilayer films composed of successive monolayers of the polyoxometalate 12-phosphotungstic acid ($H_3PW_{12}O_{40}$) and 1,12-diaminododecane (DD, $H_2N(CH_2)_{12}NH_2$) have been prepared using the LBL method (fig. II.3.1) The preparation of the (POM-DD)$_n$ multilayer film was analyzed by UV-Visible spectroscopy following the characteristic POM spectrum, and specifically its characteristic 267nm-peak.

These films were electrically characterized in different ways: a) Capacitance and leackage current measurements of vertical structures (Al/POM layer/Si(p doped)/Al), b) Current voltage measurements of planar structures (Au electrodes 50nm apart), and c) STM measurements of vertical structures (STM probe/POM layer/Si(n++ doped)/Al). In the case of capacitance measurements the application of the standard MOS analysis in this region allowed the determination of the flat band voltage shift, which is caused by the charge accumulated in the molecular layer. Current measurements are discussed in terms of tunneling mechanisms (fig. II.3.2).

Task 2 Transport properties of Cyclodextrin/Au nanoparticle host/guest systems

N.Glezos, D. Maffeo,[1] K.Yannakopoulou[1] and I.M.Mavridis[1]
[1]Institute of Physical Chemistry, NCSR “Demokritos”

The aim of this work is to fabricate nanodevices based on the transport properties of composite organic/Au nanoparticle systems. In this case, cyclodextrin derivatives bearing long aliphatic sulfide substituents were synthesized at the institute of Physical Chemistry. The derivatives feature (a) not-easily oxidizable sulfides (as opposed to thiol-groups which are prone to oxidation to sulfoxides or even sulfones), which offer seven points of attachment to the Au surface and (b) the -S- groups are connected to the cyclodextrin ring through a 10-carbon spacer, providing ample flexibility for structural organization during the deposition on the gold surface. Attachment of these molecules on Au surfaces was confirmed by RAIRS.

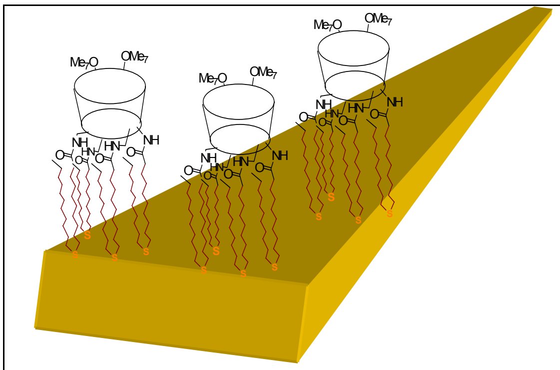


Fig II.3.3: *Cyclodextrin derivatives*

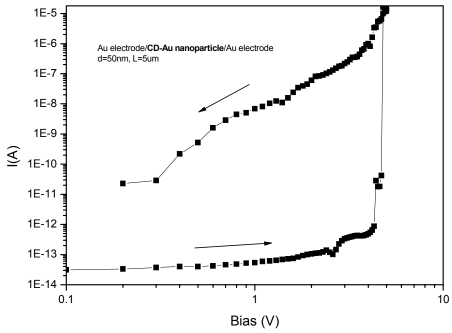


Fig II.3.4: *I-V characteristic of a composite Au nanoparticle (40nm) /CD system on Au nanoelectrodes.*

The resulting system consisted of the two nanoelectrodes (50nm) and an accumulation of Au nanoparticles bridged by the cyclodextrins. In the case of current measurements the Au nanoparticles act as donors/acceptors of electrons with different potential in each case. The system is reversibly charged/uncharged (fig. II.3.4) showing instability when the applied voltage is decreased. Further work will focus on the functionalisation of the nanoparrticles with selected organic guests for the cyclodextrin host.

Task 3 Evaluation of organic crystals for OTFT applications

G.Chaidogiannos, N.Glezos, , S. Kennou[2], F. Petraki[2], S. Nespurek[3]
[1]Institute of Physical Chemistry, NCSR “Demokritos”
[2]Department of Chemical Engineering, University of Patras
[3]Institute of Macromolecular Chemistry, Academy of Sciences of the Czech Republic

Organic thin film transistors (OTFTs) have already been used in diverse applications such as electronic paper, chemical sensors, radio frequency tags and memory devices. Pentacene and α-sexithiophene are the molecular materials with the highest reported field mobilities as p-channels in OTFTs. However both materials present processing difficulties due to their limited solubility. Metal phthalocyanines (MePc) is another class of compounds which has been investigated for the same purpose. Their advantages are their chemical and thermal stability (stable up to 400°C, easily vacuum evaporated). Their field mobilities in transistor structures are of order 0.01 $cm^2/V.s$ (for CuPc). Recently, the mobility value of 1 $cm^2/V.s$ for CuPc single crystals was reported. Sulfonated MePcs (Me = Co or Zn, Cobalt or Zinc phthalocyanine; mixtures of monosulfo and disulfo derivatives) were either synthesized by the Czech group, or purchased and purified.

Both spin coating and vacuum evaporation were used for the film preparation. The knowledge of the barrier heights at interfaces between the electrodes and the active organic layers is of great importance for understanding and improvement of organic semiconducting devices. The electronic structure of the metal phthalocyanines/ Au interface was investigated by X-ray and UV Photoelectron spectroscopies in the University of Patras. The band energy diagram of the interface was obtained in this way, from which the hole and electron injection barriers can be determined.

The transistor structures consist of source-drain Au electrodes on a Si (n++)/SiO_2 substrate with an Al backgate. Using interdigitated electrode geometries with gate lengths L = 2, 5, 10 and 30μm and channel width W in the millimeter range, ratios W/L ~10^3 were obtained.

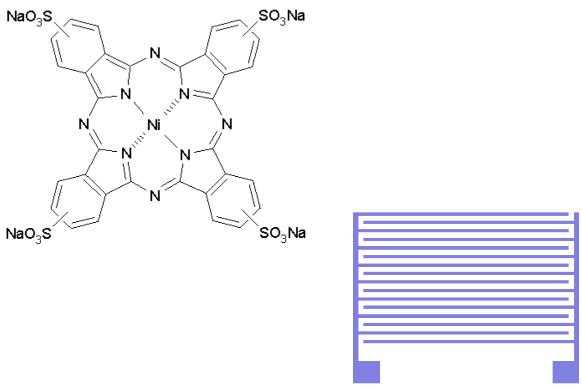


***Fig. II.3.5:* (a)** *Example of sulfonated Ni -PCs* **(b)** *Electrode geometry. Electrode size 1mm, interelectrode spacing 2-30μm.*

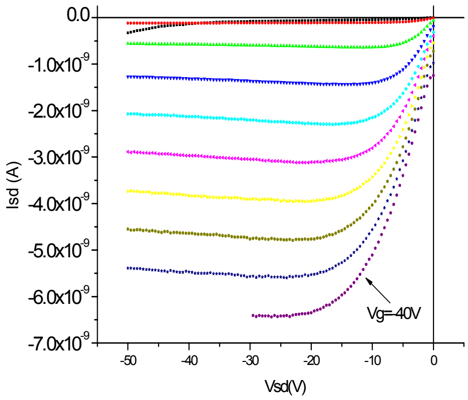


Fig II.3.6: *Characteristics of an unsulfonated Ni –Pc, p type transistor prepared by sublimation. Film thickness 30nm and electrode distance 30μm.*

Task 4 Transport properties of nanostructures.

N.Papanikolaou , H. Ebert, I. Mertig

The last years witnessed an increased interest in investigating the spin-dependent transport between two ferromagnetic electrodes separated by either an insulator or a semiconductor, systems now commonly known as magnetic tunnel junctions MTJs. Generally a realistic geometry is required for theoretical investigations on the magnetoresistance to enable a sensible comparison between theory and experiment. Most of the theoretical investigations, however, treated the two spin subsystems participating in the conduction independently, two-current model, introducing this way a spin filter. The transport is treated either on the basis of the Kubo-Greenwood or on the Landauer-Büttiker formalisms. We have performed fully relativistic calculations and presented a detailed analysis on how spin-orbit coupling influences the conductance by mixing the different spin channels.

Another interesting field is electronic transport through atomic size constrictions. Small, few atom molecules are attached to metallic leads and the electronic conductance is calculated using the Bandauer formalism. The electronic structure of the molecule including the metallic lead are calculated using ab-inito calculations based on density functional theory. Our study is focused on the influence of the chemistry of the contact the bonding to the leads and the geometry of the contact to the transport properties

Task 5 Magnetic properties of II-VI dilute magnetic semiconductors.

N.Papanikolaou and K. Trohidou

Over the recent couple of years, Mn-doped III-V and II-VI diluted magnetic semiconductors (DMS) have become an important playground for developing our understanding of carrier-mediated magnetism in solids. To a large extent, this stems from the fact that in these systems the relevant interactions can be tuned by changing the carrier and magnetic ion densities as well as by imposing strain, confinement, electric field, or illumination. Monte Carlo simulations we employed to assess the influence of magnetization fluctuations, short-range antiferromagnetic interactions, disorder, magnetic polaron formation, and spin-Peierls instability on the carrier-mediated Ising ferromagnetism in two-dimensional electronic systems. The determined critical temperature and hysteresis are affected in a nontrivial way by the antiferromagnetic interactions. The findings explain striking experimental results for modulation-doped p-Cd1-xMnxTe quantum wells.

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS

1. “Tungstate poloxometalates as active components of molecular devices”, D.Velessiotis, N.Glezos and V.Ioannou-Sogleridis, Journal of Applied Physics, 98 (8),084503 2005
2. “Monte Carlo Simulations of Ferromagnetism in p-Cd(1-x)Mn(x)Te Quantum Wells”, D. Kechrakos, N. Papanikolaou, K.N. Trohidou, and T. Dietl, Phys. Rev. Lett. 94, 127201 (2005)
3. “Influence of spin-orbit coupling on the transport properties of magnetic tunnel junctions”, V. Popescu, H. Ebert, N. Papanikolaou, R. Zeller, and P. H. Dederichs, Phys. Rev. B 72, 184427 (2005)
4. “Electronic transport through atomic size constrictions”, N. Papanikolaou A. Bagrets, I. Mertig, J. Phys. Conf. Ser. 10 109 (2005)

PRESENTATIONS in CONFERENCES

1. “Electronic transport properties of organic/inorganic composite materials in the nanoscale”, N.Glezos (Invited talk), Nanomeeting 2005, Minsk
2. “Electrical characterization of molecular monolayers containing tungsten polyoxometalates” , N.Glezos, Douvas A. M., Argitis P. , Saurenbach F., Chrost J., Livitsanos C., MNE Conference, Vienna

PROGRAM III
SILICON SENSORS and MICROSYSTEMS

Programme representative: Dr C. Misiakos

General

Program III targets the development and use of state of the art silicon micromachining and other micro and nanofabrication techniques, as well as physico-chemical functionalization technology in the fabrication of novel sensor devices. The development of microsystems (MEMs) using these sensors is another target of this program. The field of microsystems and sensors constitutes a technological area with a very important economic impact in the coming years. It is so considered by IMEL as a strategic area of paramount importance for the country.

Research activities within program III are the following:

- Porous silicon technology for sensors and on-chip integration
- Mechanical and Chemical Sensors
- Bio–Microsystems
- Thin film devices for large area electronics
- Circuits and Devices for optoelectronic interconnects

IMEL started the activity in this field at the early nineties. It concentrated its efforts in developing enabling technologies and a pool of novel products and proprietary processes, in order to pave the way towards the development of an industrial activity in Greece in the field of MEMs. Important collaborations with industry were developed so far.

IMEL also developed a strong international partnership through its collaboration in a large number of competitive EU research projects, contracts with industry and contracts with the European Space Agency, Eureka/Eurimus program etc. It also developed collaboration in critical interdisciplinary technologies with other NCSR ”D” Institutes.

Project III. 1: POROUS SILICON TECHNOLOGY and APPLICATIONS

Project leader: Dr A. G. Nassiopoulou
Key Researchers: Dr A. G. Nassiopoulou and Dr H. Contopanagos
Post-doctoral scientist: Dr D. Pagonis, Dr D. Goustouridis (part time)
Phd students: F. Zacharatos, V. Gianneta
Collaborating researcher: Dr G. Kaltsas

Funding:

- EU Marie Curie/ ''RF on porous'', re-integration grant, Contract N^0 016142, 29/7/2005-28/7/2007
- Contract from the National Research Agency-Cyprus, Photothermal analysis, 1/7/2004-30/6/2006
- Contract with the company Unilever UK, Flow system for Unilever, 1/12/2005-31/5/2007
- Contract with the company ST Microelectronics SA France, RF-on-porous, 30/7/2005-30/7/2008

Research orientation:

- Material development (Nanoporous or macroporous silicon)
- Development of micromachining processes
- Application in flow sensors, accelerometers, microfluidic devices and on-chip integration of RF components.

a) Porous silicon technology for sensors

A big effort has been devoted the last years at IMEL in developing enabling processing technologies and materials for different applications including sensors and systems. One such technology with important potential for applications is porous silicon technology.

Porous silicon is a nanostructured material which may be formed locally on a silicon substrate by electrochemistry. It presents high thermal and electrical resistivity and it may be used as a micro-hotplate material in silicon thermal sensors. In addition, porous silicon shows etching selectivity compared to bulk silicon and it is a very good sacrificial material for bulk silicon micro-machining.

Important expertise and know how on porous silicon have been developed at IMEL within different EU and national projects, as well as within direct contracts with industry, including:

- Proprietary micromachining techniques based on the use of porous silicon as a sacrificial layer for the fabrication of free standing silicon membranes, bridges and cantilevers on silicon
- Technologies using porous silicon for local thermal isolation on a silicon wafer, for RF isolation or as a matrix for the deposition of catalytic materials for chemical sensors

b) RF integration on porous silicon

This activity started at IMEL in 2004 with the overall objective:

- to explore and extend porous silicon technology into the domain of CMOS-compatible integrated RF systems for use in systems-on-chip and
- to improve the performance of currently integrated analog CMOS components by above technology transfer and related optimization of design methodologies.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Macroporous silicon

D. N. Pagonis, F. Zacharatos and A. G. Nassiopoulou

A process for the formation of both ordered and non-ordered macroporous silicon has been developed (fig. III.1.1a & III.1.1b). The resulting structure consists of an array of vertical pores perpendicular to the silicon substrate. The diameter of the developed pores is in the range of 1 to 10 micrometers depending on the type (non-ordered or ordered) of the macroporous silicon formed. The thickness of the macroporous layer can exceed 100 μm. On-going research involves the development of appropriate masking techniques for the confined formation of both types of macroporous silicon locally on a particular area of the silicon substrate.

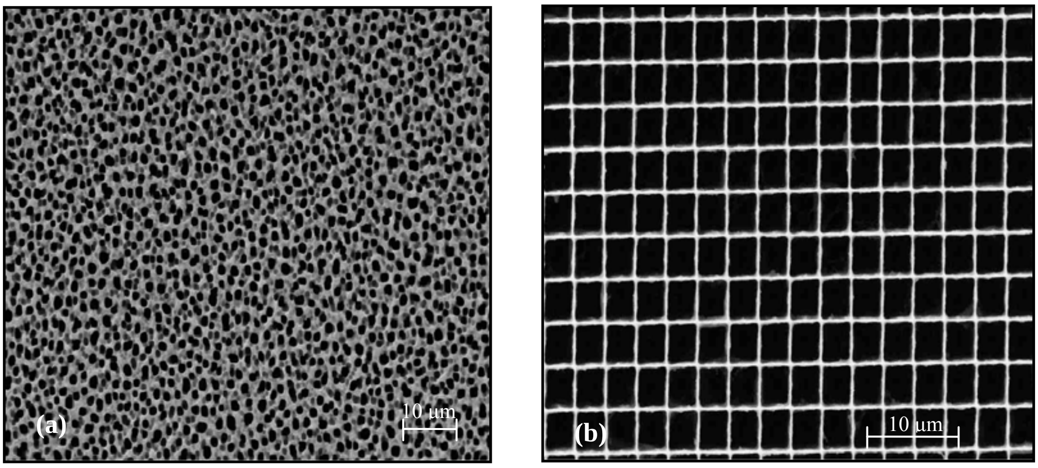


Fig. III.1.1: *SEM image of a typical non-ordered macroPS layer formed on a p-type silicon substrate. In* ***(a)*** *we see a top view, while in* ***(b)*** *a cross-sectional view of the structure. The thickness of the layer is about 9.5 μm.*

A technique for the formation of double porous silicon layers of different pore morphology has also been developed. The resulting structure consists of a layer of macroporous silicon situated above a nanoporous silicon one (fig. III.1.2a). The pore diameter of the layer underneath is in the nanometer scale. Furthermore, by proper selective wet-etching, the nanoporous silicon can be removed, resulting in a free-standing macroporous silicon membrane (fig. III.1.2b). The depth of the cavity situated underneath the membrane is directly proportional to the thickness of the nanoporous silicon layer, formed at a previous stage of the process.

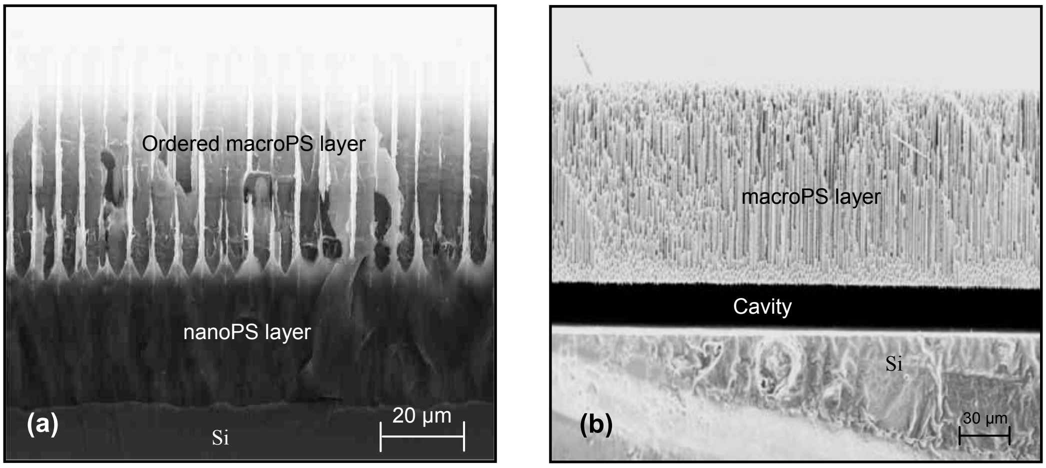


Fig. III.1.2: *Cross-sectional SEM images of typical structures consisting of macroporous silicon over nanoporous silicon before* ***(a)*** *and after* ***(b)*** *the selective etch of the nanoporous layer.*

Task 2 Flow sensor with microfluidic channel

D. N. Pagonis, A. Petropoulos, G. Kaltsas and A. G. Nassiopoulou

This work concerns the fabrication, modeling and characterization of a novel microfluidic flow sensor using porous silicon technology for the fabrication of the microfluidic channel (fig. III.1.3). The novel microfluidic flow sensor is compatible with Si technology, thus allowing for integration on the same chip of the appropriate read-out electronics. The microchannel is sealed by a porous silicon membrane, thus the final structure is co-planar with the rest of the substrate.The fabrication technology of buried microchannels in silicon using porous silicon technology has been developed in a previous work; the technique is based on two consecutive steps of anodization and electropolishing of p-type silicon.The sensor's basic components are the buried microchannel, a central heater and appropriate temperature sensing elements, all integrated on top of the channel.

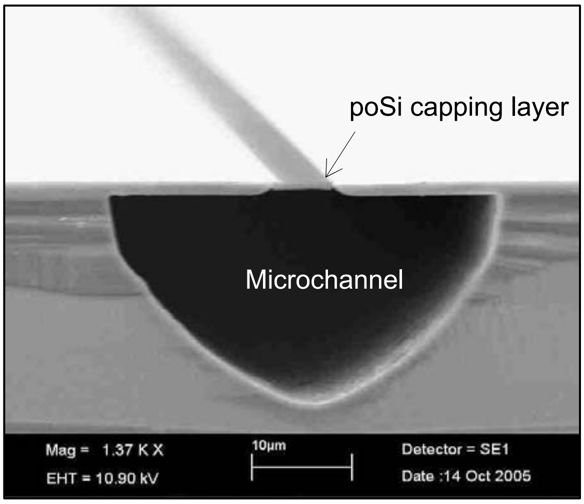


Fig. III.1.3: *SEM picture of the cross-section of the microchannel of the microfluidic sensor. The thickness of the capping nano-porous silicon layer is about 1 µm, while the depth of the cavity underneath is about 20 µm.*

The principle of operation of the device can be simply described as follows: assuming there is no liquid flow inside the microchannel, a symmetric thermal distribution is developed on top of the capping layer in the immediate vicinity of the heater. When flow is present, appropriate resistors which are integrated at both sides of the heater detect the asymmetry of the thermal distribution, induced from the flow of the liquid in the channel. The inlet and outlet of the device are situated at the two ends of the buried channel. A typical simulation result of the developed liquid flow inside the microchannel is shown in fig. III.1.4; general characteristics of the flow can be derived from modeling results. Current on-going research includes the characterization of the device.

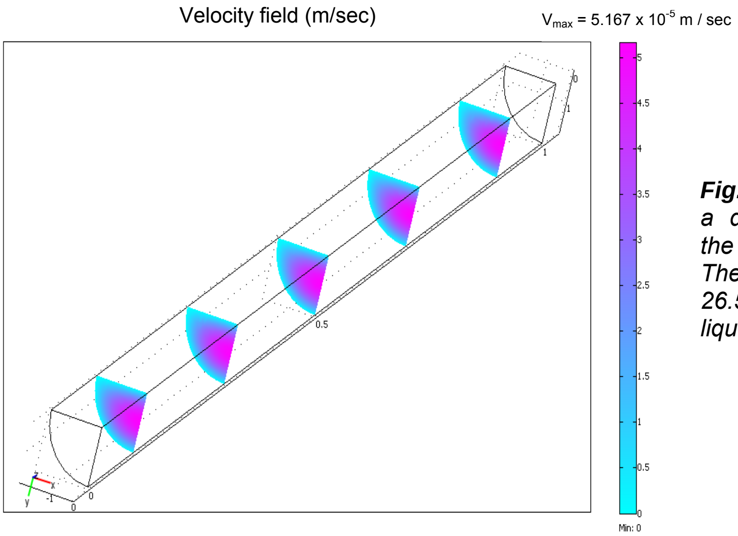
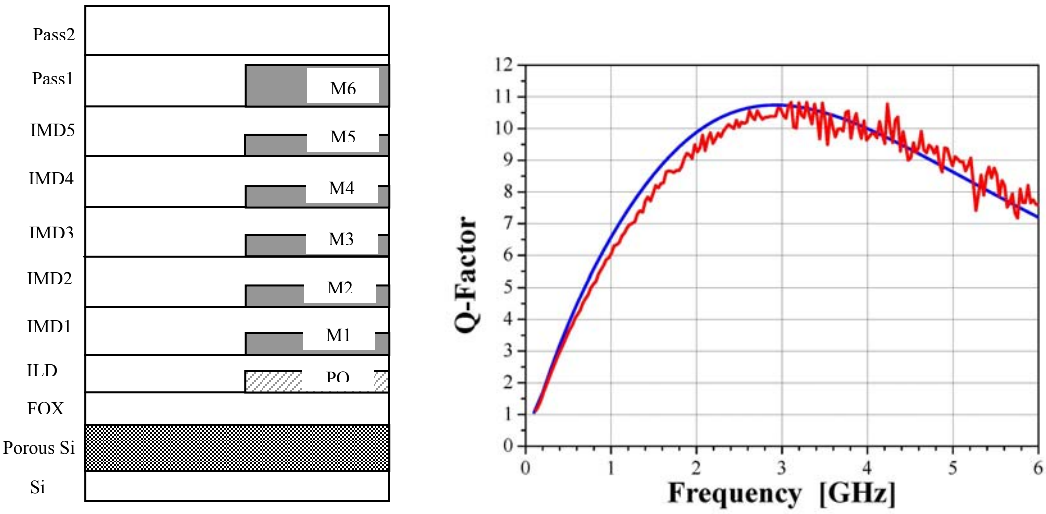


Fig. III.1.4: *Simulation results for a developed water flow inside the microchannel of the sensor. The value of the inlet velocity is 26.5 µm/sec, corresponding to a liquid flow of 1 nanoliter / min.*

Task 3 Integrated inductors on Porous Silicon in CMOS-compatible processes

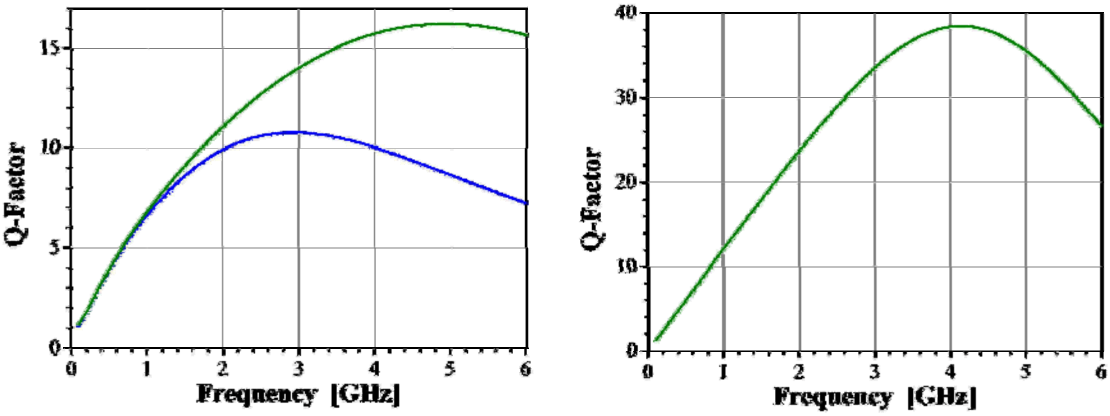
H. Contopanagos, D. Pagonis and A. G. Nassiopoulou

Radio-frequency (RF) components such as inductors, capacitors, transformers and other resonators, integrated on-chip, are essential building blocks of all analog radio frequency integrated circuits (RFICs) and their performance at current and future CMOS processes is a major bottleneck to successful system integration. It is clear that fully on-chip inductors in a CMOS-compatible process substantially improving the current art could create an important competitive advantage in the overall performance/cost ratio compared to hybrid technologies. In this work we propose the use of porous silicon as a compact micro-plate with low RF losses, grown locally on the silicon substrate by electrochemistry, as a way to implement significantly higher-Q RF inductors on a standard CMOS technology. We have first assessed the use of porous silicon isolation technology in combination with a standard CMOS technology by a) developing simulation-based inductor designs on 0.18μm CMOS technology and validating these simulations by comparison to measurements (fig. III.1.5) and then by b) extracting through simulation the inductor characteristics (same layout) when the silicon substrate is replaced by a porous silicon layer of a given thickness, dielectric constant and loss tangent (fig. III.1.6a). We find Q-factor enhancements of 50% or more in that technology.



(a) (b)

***Fig. III.1.5: a)** Typical 0.18μm 6-metal CMOS interconnect diagram and Porous Si layer, **b)** Q-factor of a 5-metal-layer inductor on 0.18μm CMOS without Porous Si: Blue=Theoretical, Red=Measurements.*



(a) (b)

***Fig. III.1.6: a)** Simulated Q-factor of the inductor of fig.III.1.5 without Porous Si (Blue) and with porous Si (Green). **b)** Simulated performance of an optimized 2-metal Cu inductor compatible with CMOS 0.13μm technology.*

PROJECT OUTPUT in 2005

PUBLICATIONS in REFEREED JOURNALS

1. “Electronic structure of C60, CuPc and C60/CuPc nanoparticles and their layers”, I. Lysko, A. Gorchinskiy, E. Buzaneva, C. Tsamis, A. G. Nassiopoulou, P. Scharff, L. Carta-Abelmann, K. Risch, Fullerenes, Nanotubes and Carbon Nanostructures 13(3), 259 (2005)
2. "Porous Si for sensor applications", A. G. Nassiopoulou (invited paper) in "Nanostructured and Advanced Materials", edited by: A. Vaseashta, D. Dimova-Malinovska and J. M. Marshal, NATO Science Series II. Mathematics, Physics and Chemistry, vol. 204, pages 189-204, (2005)
3. “Investigations by X-ray topography of quartz and lengasite resonators”, I. Mateescu, B. Capelle, J. Detaint, G. Johnson, E. Tsoi, C. Bran, J. Phys. IV France 126 (2005) 3-6

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Generation of guided terahertz electromagnetic waves in semiconductor superlattices”, R. H. Tarkhanyan and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 19-22 (2005)
2. “Combination of integrated thermal flow and capacitive pressure sensors for high sensitivity flow measurements in both laminar and turbulent regions”, G. Kaltsas, D. Goustouridis, A. G. Nassiopoulou and D. Tsoukalas, J. Phys.: Conf. Ser. 10 277-280 (2005)
3. “A microcontroller-based interface circuit for data acquisition and control of a micromechanical thermal flow sensor”, P. Asimakopoulos, G. Kaltsas and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 301-304 (2005)
4. “Stress characteristics of suspended porous silicon microstructures on silicon”, K. Anestou, D. Papadimitriou, C. Tsamis and A. G. Nassiopoulou, J. Phys.: Conf. Ser. 10 309-312 (2005)
5. “Metamorphic Electromagnetic Media”, C. Kyriazidou, H. Contopanagos and N. Alexopoulos, Proceedings of the 9th Intern. Conf. On Electromagnetics in Adv. Applications ICEAA 2005 (September 2005), Torino, Italy, pp. 965-968.
6. “Electromagnetic design methods in systems-on-chip: Integrated filters for wireless CMOS RFICs”, H.Contopanagos, Journal of Physics, Conference Series, Vol.10, 2005, pp. 337-342.

INVITED TALKS

1. “More than Moore: Technologies for Nanoelectronics, MEMs and other emerging applications”, Androula G. Nassiopoulou, ISNM 2005 (Third International Symposium on Nanomanufacturing), Limassol. Cyprus, November 3-5, 2005
2. “Embedded Antennas and Matching Networks in wireless communications”, H. Contopanagos, WSEAS International Conference on Engineering Education, July 8-10 2005, Athens, Greece.

CONFERENCE PRESENTATIONS

1. “Study of a Novel Thermal Accelerometer System”, G. Kaltsas, D. Goustouridis and A. G. Nassiopoulou, Eurosensors XIX, Barcelona, Spain, Sept. 11-14, 2005.
2. “Macroporous silicon with regular arrays of vertical pores on p-type wafers”, D. N. Pagonis, J. Semai and A. G. Nassiopoulou, XXI Panhellenian Conference on Solid State physics and Materials Science, Nicosia, Cyprus 28-31 August 2005
3. "Technology for the formation of Macroporous silicon over Cavity", D.N. Pagonis, J. Semai and A.G. Nassiopoulou, International Conference on Micro and Nano Engineering, Vienna, Austria19-22 Sept., 2005
4. "Free-Standing Macroporous Silicon Membranes Over Nanoporous/Cavity by Electrochemical Process" , D. N. Pagonis, J. Semai and A. G. Nassiopoulou, 3rd International Symposium on Nanomanufacturing (ISNM 2005), Nicosia, Cyprus, November 3-5, 2005
5. “Metamorphic Electromagnetic Media”, 9th International Conference On Electromagnetics in Advanced Applications ICEAA 2005, September 12-16 2005, Torino, Italy.

EDITION of CONFERENCE PROCEEDINGS

1. Edition of the Proceedings of the International conference of PSST on Porous Semicondictor Science and Technology, held in Cullera-Valencia, 14-19 March 2004, Special Issue of Physica Status Solidi, Guest editors: L. Canham, A. G. Nasiopoulou, and V. Partkhutic, Wiley-VCH, (2005)
2. Proceedings of the Second International Conference on Microelectronics, Microsystems and Nanoelectronics (MMN), held at NCSR Demokritos in Athens on 14-17 November 2004. Special issue of the Institute of Physics: Conf. Series (Editors: A. G. Nassiopoulou, N. Papanicolaou, C. Tsamis). Published also on-line at jpconf.iop.org (2005)

Project III. 2: MECHANICAL AND CHEMICAL SENSORS

Key Researchers: Dr C. Tsamis, Dr I. Raptis, Dr P. Normand

Post-doctoral scientists: Dr S. Chatzandroulis, Dr D. Goustouridis

Phd students: R. Triantafyllopoulou,

Collaborating researchers from other projects: Dr A. Tserepi

External Collaborators: Dr D. Papadimitriou (NTUA), Dr M. Sanopoulou (IPC, NCSR ‘ Demokritos’), Dr K. Beltsios (Materials Sci. Dept. Uni. Ioannina), Prof. D. Tsoukalas (NTUA)

Funding:

- EU, IST, IP, GOODFOOD, “Food Safety and Quality Monitoring with Microsystems”, Contract N^{o} 508774, 1/1/2004-30/6/2007
- GSRT-PENED 03ED630, “Micromachined chemical sensors for controlling food safety and quality”, 1/11/2005-1/11/2008
- GSRT- ENTER 05EP032, “Development of MOSFET type chemical sensors for wireless sensor networks”, 1/12/2005-1/12/2007
- Industrial Cooperation with Remon Medical, 1/6/2001-31/5/2002 (31/12/2006)

Research orientation:

- Development of micromachining processes for the realization of novel chemical and mechanical sensors.
- Development of low power silicon sensors based on new materials and new processes
- Design, fabrication and testing of microsystems using silicon sensors.
- Realization of sensors for specific industrial applications with emphasis on medical, food and automotive fields.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Alternative micro-hotplate design for low power metal-oxide (MOX) sensor arrays

R. Triantafyllopoulou, C. Tsamis, S. Chatzandroulis and A. Tserepi*
Contact person, e-mail: ctsamis@imel.demokritos.gr

One major requirement for the fabrication of low power sensors, especially for integration in arrays, is the reduction of thermal losses. This can be achieved by the fabrication of the active elements of the sensors on suspended structures (micro-hotplates). Two different types of micro-hotplates have been used in the literature: The *closed-type membrane*, where the membrane overlaps the silicon substrate along its periphery and the *suspended-type* membrane, where the membrane is supported on the Si substrate by means of supporting beams. In the latter case, the thermal losses to the substrate take place only through the supporting beams, and thus they are minimized compared to the closed type membrane.

During this year we performed design and optimization of suspended micro-hotplates, using two alternative technologies: a) *silicon-nitride technology* (fig III.2.1a) and b) *porous silicon Technology* (fig III.2.1b). Release of the micro-hotplates is performed by dry or wet techniques. There is one important advantage to use porous silicon as material for the micro-hotplates. Since the thermal conductivity of porous silicon is very low, *thicker* micro-hotplates can be fabricated, with improved mechanical characteristics, compared to the thin and more fragile nitride/oxide membranes. This permits us to implement *alternative* micro-hotplate designs (fig III.2.2a), with two or even one supporting beam (fig. III.2.2b).

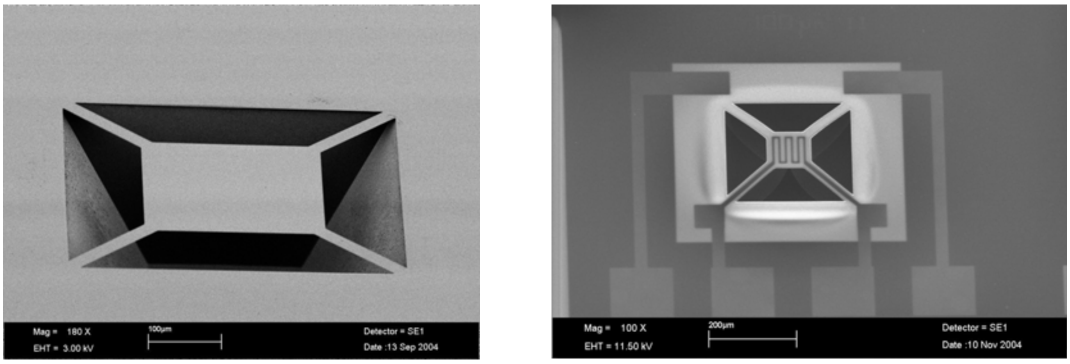


Fig. III.2.1: ***(a)*** *SEM image of a silicon nitride membrane released with wet etching of the substrate in TMAH solution,* ***(b)*** *SEM image of a Porous Silicon micro-hotplate, with integrated heater and electrodes, released with dry etching. Both micro-hotplates have four supporting beams.*

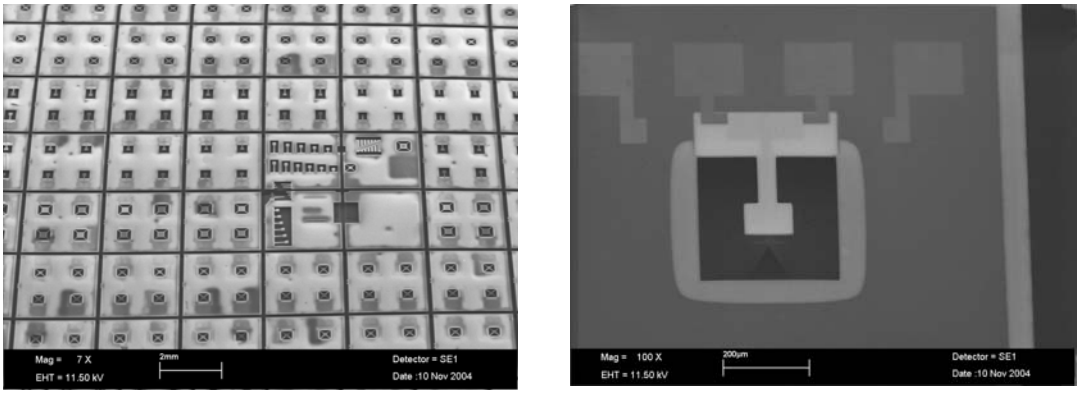


Fig. III.2.2: ***(a)*** *Fully processed wafer that contains various alternative micro-hotplate designs with four, two and one supporting beam, for improved thermal isolation,* ***(b)*** *SEM image of a Porous-Silicon cantilever-type micro-hotplate, with one supporting beam.*

Task 2 Electronic ASIC for MOX Chemical Sensors

*P. Robogiannakis, S. Chatzandroulis** *and C.Tsamis*
**Contact person, e-mail: stavros@imel.demokritos.gr*

The correct operation of metal oxide (MOX) sensors requires precise control over the operating temperature of the device simultaneously with the read-out of the chemically sensitive resistance. To this end, an electronic ASIC (fig. III.2.3) has been developed able to interface a quad gas sensor array to a microcontroller and thereon to a PC or E-nose system. The chip contains in a single IC all the necessary analog electronics to operate four MOX sensors while the control logic will be implemented on the microcontroller (fig. III.2.4). The ASIC has been successfully implemented in a single-poly, double-metal, 0.7μm CMOS process (fig. III.2.3) and first measured results are in agreement with simulated values. Provision has been taken for both polysilicon and Pt heater control.

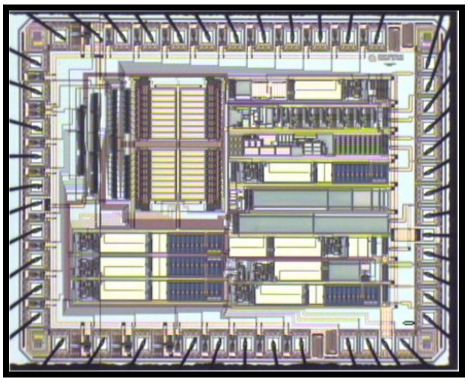


Fig. III.2.3: *Fabricated ASIC chip*

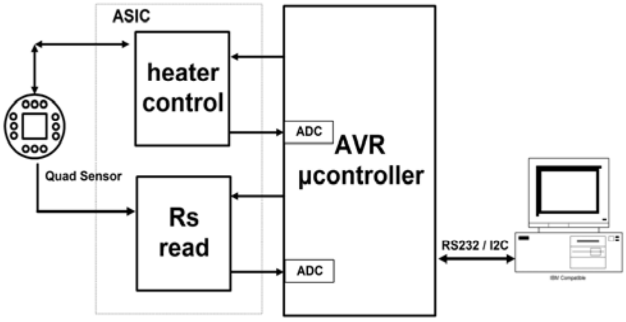


Fig. III.2.4: *Schematic of the MOX electronic control system.*

Typically the sensitive element of MOX sensors consists of a semiconductive metal-oxide layer whose resistance is a function of the concentration of specific gases in the sensor ambient and could range from a few hundred Ohms up to several MOhms, depending on the catalytic material used. The read-out circuit measures the resistance of each sensitive element in the quad sensor array by forming a voltage divider between the sensor and one of the internal on-chip resistors. The signal is then filtered and amplified before being made available for off-chip sampling by one of the 10-bit ADCs of the AVR (fig. III.2.5). The temperature control circuit provides the necessary heating power to each of the four micro-heaters until they reach the ideal operation temperature. Heater resistances are known to vary between a few Ohms up to a few KOhms depending on the heater material used. Therefore, the output of each D/A converter is fed to a buffer, which either drives the heater directly or through a high current external buffer for the case of low resistance Pt heaters.

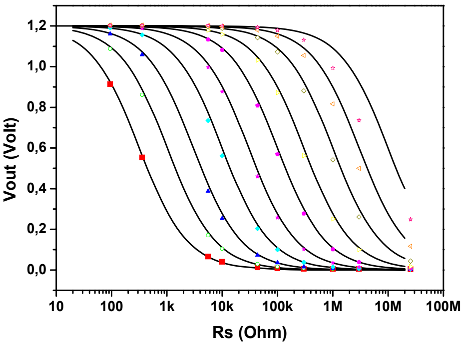


Fig. III.2.5: *Simulated R_s (line) versus measured R (symbols) resistance sweep (100 Ohm to 20 MOhm).*

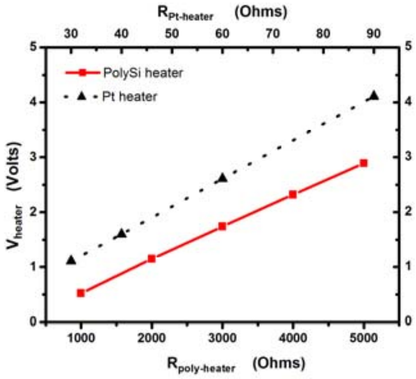


Fig. III.2.6: *Heater Resistance Circuit Response*

Task 3 Materials and processes for polymer based chemical sensors

M.Kitsara, K.Manoli, D.Goustouridis, S.Chatzandroulis and I.Raptis[*]
[*]*Contact person, e-mail: raptis@imel.demokritos.gr*

A simple process to deposit up to four polymers in selected areas to be used as sensitive layers in chemical sensor arrays was developed. The process (fig. III.2.7) is based on photolithographic processes and takes advantage of the balance between UV exposure dose, material tone and developers used. Furthermore, the discriminating capability of the constructed array is further expanded by engineering the sensing properties of two of the deposited polymers by selective exposure to DUV irradiation. The sensing properties of the deposited films in the array were characterized by monitoring in situ the volume expansion upon exposure to volatile organic compounds using white light interferometry (fig. III.2.8). The swelling properties of processed films were compared to the unprocessed ones for the purpose of examining the variation induced by the exposure and development circles and was found to be negligible. The lithographic process developed offers good control of the lateral dimensions and the thickness of the polymeric films and facilitates the fabrication of sensors operating with different transduction mechanisms including mass sensitive and stress induced bending chemical sensors.

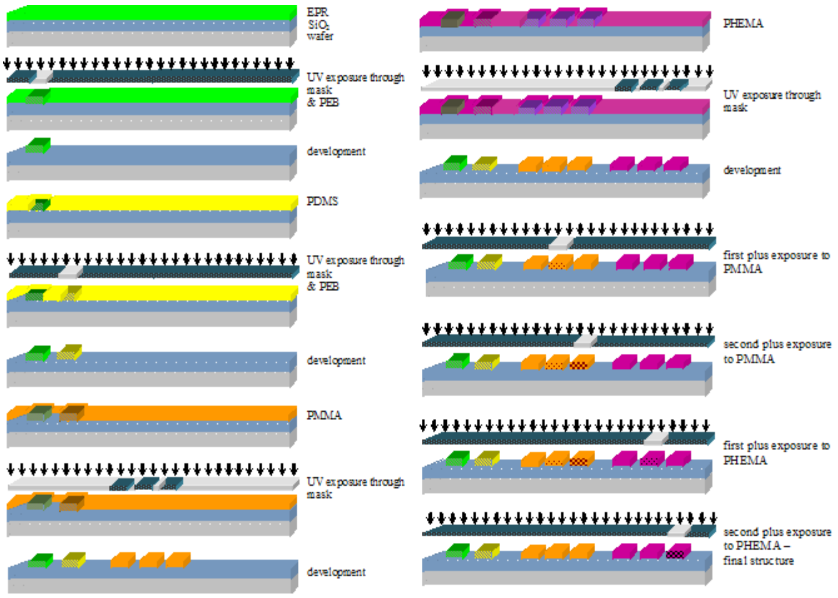


Fig. III.2.7: *Fabrication flowchart of the polymer array and processing*

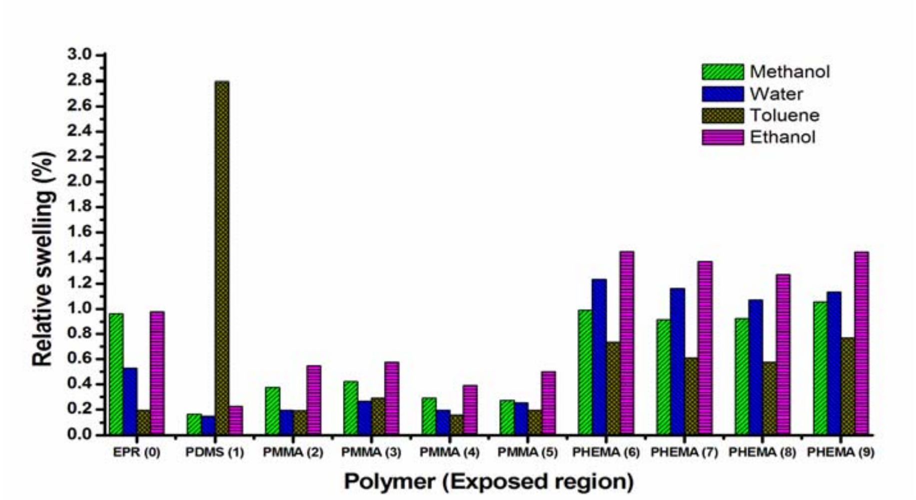


Fig. III.2.8: *Relative swelling of all polymer regions. The numbering of each polymer is in accordance with the configuration in fig. III.2.7.*

Task 4 Capacitive Type Sensors

S. Chatzandroulis, D. Goustouridis, D. Tsoukalas and P. Normand[*]
[*]*Contact person, e-mail: normand@imel.demokritos.gr*

Pressure Sensors

In 2005 our industrial cooperation in the field of pressure sensors was carried on by involving the Institute in the development of a modified version of the capacitive-type-sensors (U.S patent 6,704,185) we produced since 1998 for new applications in the medical field.

Also in 2005 the stress induced buckling and sensor diaphragm behavior have been extensively studied by developing finite element models (see fig. III.2.9). This activity aims at evaluating the deflection of the pressure sensor diaphragm upon exposure to an external pressure differential also taking into account the stress induced due to the heavy doping with boron as well as the stress induced on the diaphragm from the various structural layers of the device.

Substantial efforts were also devoted to the fabrication of capacitive pressure switches based on the use of strain compensated heavily boron doped SiGeB diaphragms. The process relies on the silicon fusion bonding of two silicon wafers to seal the pressure sensor cavity. Pressure switches operating at different pressure thresholds have been successfully realized. Current flowing through the switch jumps over six orders of magnitude when its two plates come in contact (see fig. III.2.10)

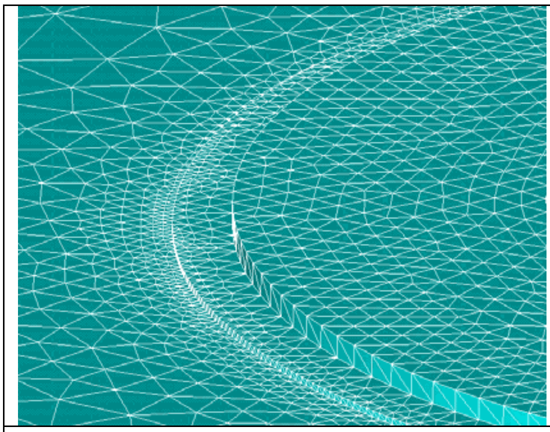


Fig. III.2.9: *Capacitive pressure sensor meshing*

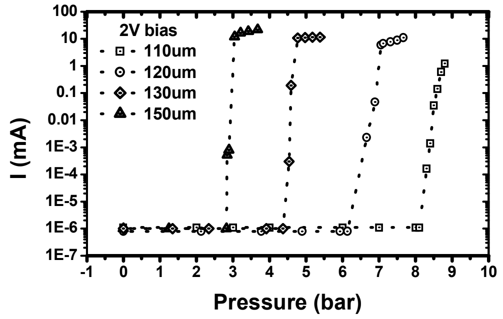


Fig. III.2.10: *Pressure switches operating in the 3 to 8 bar range.*

Capacitive DNA Sensors Arrays

The recent deciphering of all human genes by the Human Genome Project has made apparent that the genetic determinants for most, if not all common complex diseases, including heart disease, cancer and diabetes, hypertension, hypercholesterolemia could now be identified and evaluated. As a response to these worldwide research efforts in health care, we recently oriented part of our activities to the development of DNA detector arrays based on capacitive detection. The Capacitive DNA Sensors Arrays to be developed will exploit the surface stress changes and subsequent bending of ultra thin silicon membranes induced by the receptor DNA deposited on the membrane surface (see fig. III.2.11). The membranes seal the capacitor plates from the electrolyte solution thus enabling capacitive detection. These activities will be conducted within the frame of the European Project Micro2DNA.

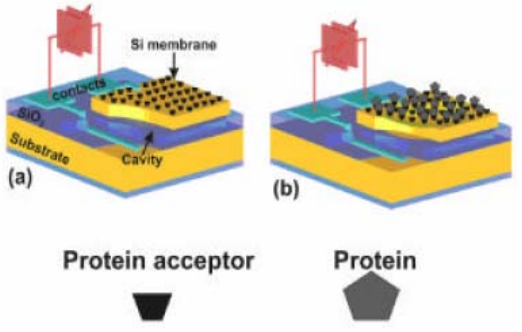


Fig. III.2.11: *Capacitive Biosensor principle*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. “Polymeric film characterization for use in bimorph chemical sensors”, S. Chatzandroulis, D. Goustouridis, I. Raptis, Microelectron. Eng. 78-79 118(2005)
2. ”Characterization of Polymer Layers for Silicon Micromachined Bilayer Chemical Sensors Using White Light Interferometry”, D. Goustouridis, K. Manoli, S. Chatzandroulis, M. Sanopoulou, I. Raptis, Sens. Act. B 111-112, 549(2005)
3. “Alternative micro-hotplate design for low power sensor arrays”, R. Triantafyllopoulou, S. Chatzandroulis, C. Tsamis, A. Tserepi, To appear in Microelectronics Engineering

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Simulation of Capacitive type Bimorph Humidity Sensors”, J. Fragakis, S. Chatzandroulis, D. Papadimitriou & C. Tsamis, J. Phys.: Confer. Series 10, 305-308,2005
2. “Characterization of polymers films for use in bimorph chemical sensor”, S. Chatzandroulis, D. Goustouridis, I. Raptis, J. Physics: Confer. Series 10, 297–300(2005)

CONFERENCE PRESENTATIONS

1. “Alternative micro-hotplate design for low power sensor arrays”, R. Triantafyllopoulou, S. Chatzandroulis, C. Tsamis, and A. Tserepi, Micro- and Nano-Engineering, MNE 2005, 19-22 September 2005, Vienna, Austria (Oral)
2. “Fabrication and characterization of Porous Silicon cantilevers for thermal sensors”, S. Chatzandroulis, C. Tsamis and A. Tserepi, SPIE Conference on “Microtechnologies for the New Millenium 2005”, 9-11 May 2005, Seville, Spain (Oral)
3. “Design and simulation of capacitive cantilever bimorph chemical sensors”, J. Fragakis, S. Chatzandroulis, D. Papadimitriou and C. Tsamis, Eurosensors XIX, Barcelona, Spain, September 11-14, 2005 (Poster)
4. “Integrated interface IC for metal-oxide chemical sensor arrays”, P. Robogiannakis, S. Chatzandroulis & C. Tsamis, Eurosensors XIX, Barcelona, Spain, Sept. 11-14, 2005(Oral)
5. “A simple process for the deposition of polymer arrays for use in chemical sensing”, D. Goustouridis, M. Kitsara, S. Chatzandroulis, K. Beltsios, I.Raptis, Eurosensors XIX, Barcelona, Spain, September 11-14, 2005 (Poster)
6. “Sorption of vapors in thin polymer films studied by white light interferometry”, K. Manoli, D. Goustouridis, S. Chatzandroulis, I. Raptis, M. Sanopoulou, 4th Int. Conf. Instrumental Methods of Analysis (Iraklion, Greece, 10/2005) (Poster)
7. “UV irradiation as a means of engineering polymer swelling properties used in chemical sensors”, D. Goustouridis, S. Chatzandroulis, I. Raptis, E.S. Valamontes, 4th Int. Conf. Instrumental Methods of Analysis (Iraklion, Greece, 10/2005) (Oral)
8. “A Lithographic Polymer Process Sequence for Chemical Sensing Arrays”, M. Kitsara, D. Goustouridis, S. Chatzandroulis, K. Beltsios, I. Raptis, Micro- and Nano-Engineering, MNE 2005, 19-22 September 2005, Vienna, Austria) (Oral)
9. “Capacitive Pressure Sensors And Switches Fabricated Using Strain Compensated SiGeB”, S. Kolliopoulou, S. Chatzandroulis, D. Goustouridis, D. Tsoukalas, Micro- and Nano-Engineering, MNE 2005, 19-22 September 2005, Vienna, Austria) (Poster)

M. Sc. THESES

1. “Optimization of suspended microhotplates for micromechanical sensors”, R.Triantafyllopoulou, SEMFE/NTUA, November 2005, Supervisor: C. Tsamis
2. “Sorption of vapors in thin polymer films studied by white light interferometry”, K.Manoli, October 2005, Supervisors: I. Raptis, M. Sanopoulou
3. “Development and Characterization of Si/polymer bimorph chemical sensors”, A.Batagiannis, September 2005, Supervisors: D.Goustouridis, D.Tsoukalas
4. “Reliability study of micromelectromechanical pressure sensors”, I.Politis, July 2005, Supervisors S.Chatzandroulis, D.Tsoukalas.

DIPLOMA THESES

1. “Characterization and modeling of suspended microstructures for sensor applications”, J. Fragakis, SEMFE/NTUA, June 2005, Supervisor: C. Tsamis
2. “Optimization of the mechanical properties of Porous Silicon for micromechanical applications”, K. Anestou, SEMFE/NTUA, July 2005, Supervisor: C. Tsamis

Project III. 3: BIO-MICROSYSTEMS

Project Leader: Dr K. Misiakos
Key Researchers: Dr A. Tserepi, Dr E. Gogolides, Dr P. Argitis
Post-doctoral scientists: Dr K. Kotsovos
Phd students: M. Vlachopoulou
Collaborating researchers from other projects: Dr I. Raptis
External Collaborators: Dr S.E. Kakabakos and Dr P.Petrou (IRRP/NCSRD)

Research orientation:

- Development of bioanalytical lab-on-a-chip devices based on monolithic optoelectronic transducers.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Multi-protein and DNA assay using chromophore labels

a) Protein Coating

The monolithic silicon micro-optical transducer employed in these experiments is shown in fig.III.3.1 and III.3.2. Coating was performed by applying on three different waveguides on the same chip solutions of biotinylated bovine serum albumin (BSA), mouse IgG and rabbit IgG solutions (20 mg/L in 0.05 M carbonate buffer, pH 9.2), respectively, using a microsyringe dispenser aligned on top of the optocouplers of the pretreated wafer. The wafer was placed on a x-y motorized stage under a microscope for monitoring the spotting process. The spotting solutions were incubated for 30 min at room temperature (RT). The chips were then washed with distilled water and blocked with a 10 g/L BSA solution in 0.1 M $NaHCO_3$ buffer, pH 8.5, for 30 min at RT. After washing as previously, the surface was dried under a nitrogen stream. The results of the assay on the chip spotted with the three different proteins are shown in fig. III.3.3 in real time. The anti-mouse IgG antibody, streptavidin (2 nM) and anti-rabbit IgG antibody were sequentially pumped through the fluidic system. Here, the R-phycoerythrin fluorescent labels are used as chromophore groups to absorb photons from the waveguided modes through evanescent wave interactions. The responses shown in fig. III.3.3 have the same starting point for every curve by shifting the injection moments of the respective protein in the fluidic cover. As expected, and due to the higher binding constant, the response to streptavidin of the optocoupler coated with biotinylated BSA was stronger compared to the other two despite the fact of the lower streptavidin concentration. The optocouplers coated with mouse IgG and rabbit IgG showed responces roughly proportional to the anti-mouse IgG antibody and anti-rabbit IgG antibody concentrations, respectively.

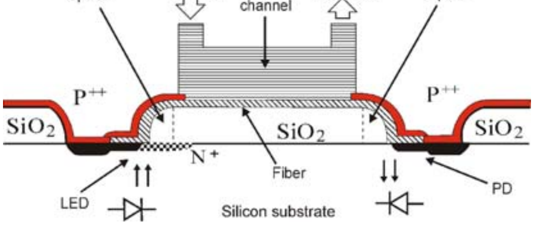


Fig.III.3.1: *Schematic Illustration of the monolithic silicon optocoupler biosensor coupled to the fluidic module*

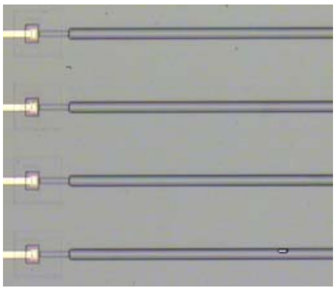


Fig.III.3.2: *Photograph of an array of optocouplers with the emitters on the left and the fiber in the middle (detectors not shown)*

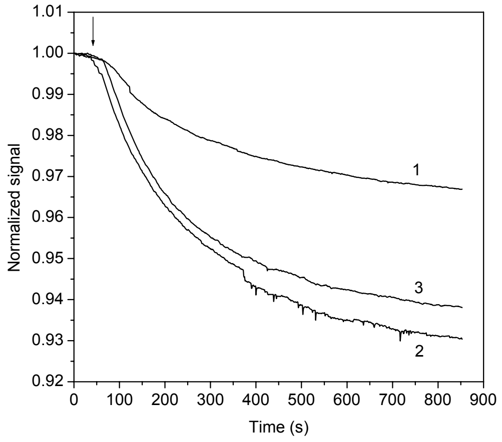


Fig. III.3.3: *Real time signal evolution obtained from three different fibers coated with mouse IgG (1), biotinylated BSA (2) and rabbit IgG (3) upon reaction with R-phycoerythrin labeled anti-mouse IgG antibody (5 nM), streptavidin (2 nM) and anti-rabbit IgG antibody (10 nM), respectively. Initial baseline was obtained by pumping through the fluidic only the assay buffer. The arrow indicates the injection of the respective labeled reagents. The signals are normalized with respect to their initial value.*

b) DNA coating

The waveguide surface was coated with a 20 mg/L biotinylated BSA solution in 0.05 M carbonate buffer, pH 9.2, for 30 min at room temperature (RT). The chips were then washed with distilled water and blocked with a 10 g/L BSA solution in 0.1 M $NaHCO_3$ buffer, pH 8.5, for 30 min at RT. After washing as previously, the surface was dried under a nitrogen stream. A biotinylated oligonucleotide (0.5 µM), corresponding to the mutant sequence of the 3099delT mutation (biotin-5'-AAACTAAAGTAAGAAAAA-3') in the BRCA1 gene, was pre-incubated with streptavidin (0.166 µM) for 30 min at a 0.05 M phosphate buffer, pH 6.5. This solution was then applied onto chips covered with biotinylated BSA and incubated for 30 min at RT. The chips were then washed with distilled water and dried under nitrogen stream. For the hybridization assay, the AlexaFluor 546 fluorophore was employed as the chromophore group. The fully complementary oligonucleotide clearly shows a photocurrent drop (fig. III.3.4) which is absent in the non-complementary oligonucleotide, and points out a good selectivity between the mutant and the wild type sequence.

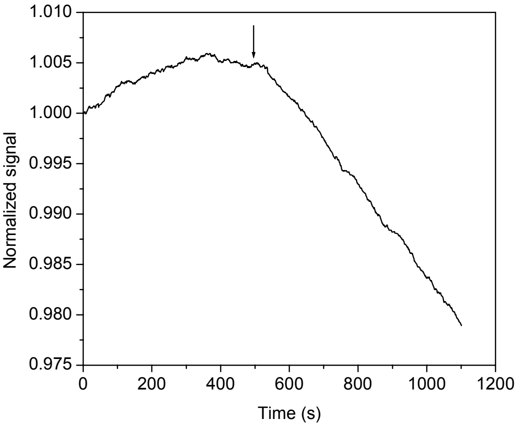


Fig. III.3.4: *DNA hybridization assay. Signal obtained in real time by pumping through the fluidics module a solution of the non-complementary oligonucleotide for approximately 500 seconds followed by injection (arrow) of the fully complementary oligonucleotide. Both oligonucleotides were labeled with AlexaFluor 546.and were used at a concentration of 0.1 µM. The signal is normalized with respect to its initial value.*

From fig. III.3.3 and III.3.4 we conclude that commercially available fluorophore groups can be employed as effective chromophores and provide bioanalytical results with the presented transducer. The selection of the particular fluors, R-phycoerythrin with AlexaFluor 546, was based on their absorption spectrum which matches, to some extent, the emission spectrum of the avalanch LEDS. Other labels with absorption peaks in the 530nm-670 nm spectral region could also be employed.

Task 2 Label-free protein assay

Here, the optocouplers were coated with biotinylated BSA so that colloidal gold-labeled streptavidin could selectively bind and give an initial photocurrent drop due to the nanoparticle plasmonic response. The amount of photocurrent drop is an increasing function of the effective refractive index of the medium that surrounds the gold nanoparticles. Consequently, if a biotinylated protein reacts with the immobilized streptaviding the gold nanoparticles will sense a slightly different medium in their vicinity which will result in a different photocurrent drop. This way the gold-labeled streptavidin is used as a capture molecule which at the same time exhibits a photon extinction cross section that depends on the molecules bound on the nanoparticle. Therefore, label free detection is possible of biotinylated biomolecules. Such a label free assay where biotinylated mouse IgG was employed as the analyte is shown in fig. III.3.5. Upon injection of the protein, the photocurrent starts dropping for about 200 seconds and then reaches a new baseline. It should be noted that this reaction proceeds at a much faster speed compared to the rates observed in fig. III.3.3. Such a trend could be attributed to the label free nature of the reaction in fig. III.3.5.

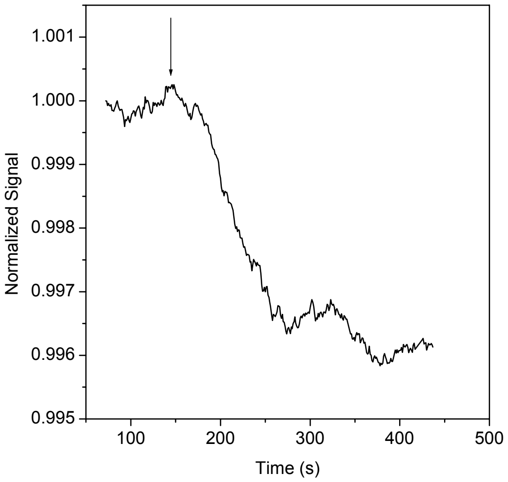


Fig. III.3.5: Label-free protein assay. Real time signal obtained from an optocoupler modified with streptavidin-gold nanoparticles conjugate. Initial baseline was obtained by pumping assay buffer (PBS) for 150 seconds with a flow rate of 20 μL/min prior to injection of biotinylated mouse IgG solution in 0.05 M PBS, pH 7.4, at a concentration of 1 nM.

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. "157-nm Laser ablation of polymeric layers for fabrication of biomolecule microarrays", Douvas, A.M., Petrou, P.S., Kakabakos, S.E., Misiakos, K., Argitis, P., Sarantopoulou, E., Kollia, Z., Cefalas, A.C., Analytical and Bioanalytical Chemistry 381 (5), pp. 1027-1032
2. "Self assembled structures on fluoro-polymers induced with laser light at 157 nm", Kollia, Z., Sarantopoulou, E., Cefalas, A.C., Kobe, S., Argitis, P., Misiakos, K., A*pplied Surface Science* 248 (1-4), pp. 248-253
3. "Patterning of thick polymeric substrates for the fabrication of microfluidic devices", Vlachopoulou, M.E., Tserepi, A., Vourdas, N., Gogolides, E., Misiakos, K., Journal of Physics: Conference Series 10 (1), pp. 293-296
4. "A bioanalytical microsystem for protein and DNA sensing based on a monolithic silicon optoelectronic transducer", Misiakos, K., Petrou, P.S., Kakabakos, S.E., Ruf, H.H., Ehrentreich-Forster, E., Bier, F.F., Journal of Physics: Conference Series 10 (1), pp. 273-276

CONFERENCE PRESENTATIONS

1. "Biochip-compatible packaging and microfluidics for a silicon optoelectronic biosensor", H.H. Ruf, T. Knoll, K. Misiakos, R.B., Haupt, M. Denninger, L.B. Larsen, P.S. Petrou, S.E. Kakabakos, E. Ehrentreich,-Foerster, F.F. Bier, 31st International Conference on Micro- and Nano-Engineering 2005, 19-22 September 2005, Vienna, Austria. Book of Abstracts MNE-2005 ID 00444 3-o_05.
2. "Monolithic silicon optoelectronic tranducers and elastomeric fluidic modules for bio-spotting and bio-assay experiments", K. Misiakos, P.S. Petrou, S.E. Kakabakos, M.E. Vlahopoulou, A. Tserepi, E. Gogolides, H.H. Ruf, 31st International Conference on Micro- and Nano-Engineering 2005, 19-22 September 2005, Vienna, Austria. Book of Abstracts MNE-2005 ID 00492 8A_02.

PhD DISSERTATION

1. "Simulation – design and fabrication of rear point contact silicon solar cells", K. Kotsovos, Department of Electrical and Computer Engineering, NTUA, June 2005

Project III. 4: THIN FILM DEVICES FOR LARGE AREA ELECTRONICS

Project leader: Dr D.N. Kouvatsos
Collaborating researchers from other projects: Dr D. Davazoglou
Ph.D. candidates: M. Exarchos, L. Michalas (University of Athens), D. Moschou, G. Kontogiannopoulos
External collaborators: Prof. G. Papaioannou (University of Athens), Dr N. Stojadinovic (University of Nis), Dr A.T. Voutsas (Sharp Laboratories of America)

Funding:

- GSRT – PENED, Development of polysilicon TFT technology with advanced techniques of film annealing and device characterization, 15/12/2005 – 14/12/2008
- GSRT-Bilateral project Greece-Serbia, Performance, stress degradation and reliability characterization of thin film transistors for the investigation of defects in polycrystalline silicon films, 5/11/2004-5/11/2006

Research orientation:

This research aims at the optimization of the active layer of polysilicon films obtained using advanced excimer laser crystallization methods and of the resulting performance parameters of thin film transistors fabricated in such films. Specifically, the targets are:

- Evaluation of device parameter (a) hot carrier and (b) irradiation stress-induced degradation and identification of ageing mechanisms in TFTs fabricated in advanced excimer laser annealed (ELA) polysilicon films.
- Investigation of effects of variations in TFT structure and fabrication process on device performance and reliability.
- Investigation of polysilicon active layer defects using transient drain current analysis in ELA TFTs.
- Investigation of the influence of film thickness and crystallization technique on defects and on device degradation for ELA technology optimization.
- Evaluation of bias stress-induced instabilities in solid phase crystallized (SPC) TFTs.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Characterization and hot carrier stress investigation

The characterization of TFTs made in sequentially laterally solidified (SLS) ELA polysilicon films has yielded systematic trends, with respect to the film thickness, in the device parameter values. For TFTs in “directional” SLS ELA films, which have very elongated grains along a preferred direction, the extracted average device parameters, as a function of the active layer thickness, are summarized in the following table:

Polysilicon Thickness (nm)	Field Effect Mobility, μ (cm²/Vs)	Threshold Voltage, V_{th} (V)	Subthreshold Slope, ***s*** (V/dec)	Domain Boundary Trap Density, N_t (cm^{-2})
30	160	-4.1	0.13	6.7×10^{11}
50	430	-1.1	0.11	4.9×10^{11}
100	580	-1.3	0.13	4.0×10^{11}

Clearly, the electron mobility increases and the estimated trap density decreases, indicating better material quality, with increasing film thickness. Furthermore, hot electron stressing measurements, to investigate trap generation and device parameter degradation, have been expanded to the case of TFTs fabricated in 50 nm thick 2^N-shot polysilicon films. This is an advanced variation of the SLS ELA technique that utilizes laser exposure through masks with many parallel slits and affords much better “grain engineering”, that is, good control of grain shapes, as well as better intragrain material quality. TFTs are subjected to DC gate and drain bias hot electron stresses under worst ageing conditions ($V_{GS} = V_{DS}/2$). In fig. III.4.1, the threshold voltage and subthreshold swing shifts ΔV_{th} and Δs, as well as the degradation of the transconductance G_m, are shown against the stressing time, for a stressing condition of (V_{GS}, V_{DS}) = (5 V, 10 V).

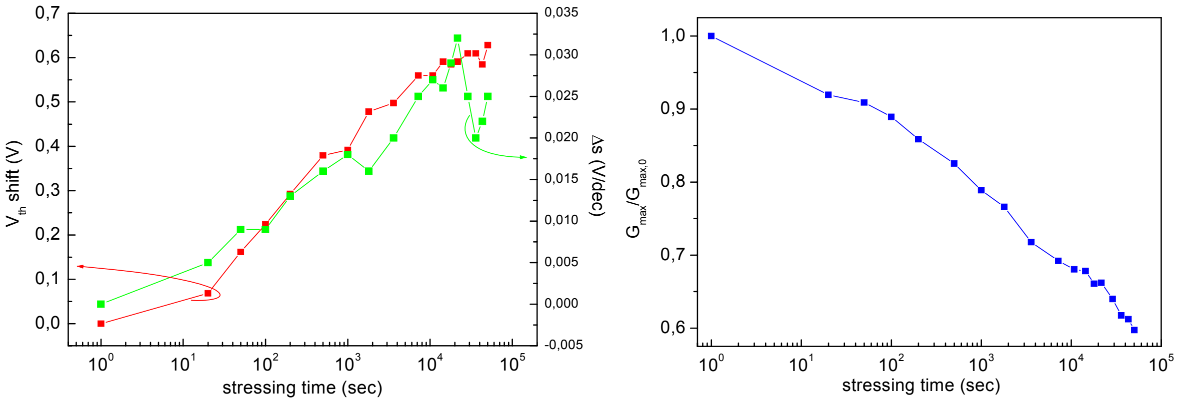


Fig. III.4.1: *V_{th} and s shifts (left) and G_m degradation (right) with stressing time for TFTs with (W, L) = (8 μm, 1.5 μm) in 2^6-shot SLS ELA polysilicon films.*

The V_{th}, *s* and g_m degradations are observed to be approximately logarithmic with stress time, indicating some active layer and interface degradation due to trap creation. The degree of degradation is similar to that earlier obtained for TFTs in directional polysilicon of the same thickness. The trap generation in the active layer is quantified, with respect to the trap density in unstressed material, by utilizing the *s* degradation.

Task 2 Transient current analysis

The drain current transients obtained in directional or 2^N-shot type SLS ELA TFTs are of the same order of magnitude at dark as well as under illumination, indicating material of high crystalline quality with low defect density. Moreover, the DLTS signals $\Delta I_{DS}/I_{DS}$ fall sharply at cryogenic temperatures, indicating a carrier generation freezeout. From these characteristics, a low concentration of generation-recombination centers and high crystallinity of ELA polysilicon films obtained by the SLS technique are inferred.

The investigation of the effect of illumination and the temperature dependence of the transient amplitude has indicated that hole emission, during the TFT ON state, is the dominant mechanism giving rise to drain current overshoot transients. The holes are generated from deep states in the device intrinsic body; those that escape recombination are captured during the OFF state and then reemitted during the ON state. At cryogenic temperatures the transient effects vanish out, as shown in fig. III.4.2, due to carrier freeze-out in deep states and exponential increase of generation lifetime. If illumination is present, electron-hole pair generation is enhanced, compensating the carrier freeze-out caused by the generation lifetime increase and leading to an extension of the transient behavior at low temperatures; thus the transient amplitudes remain high. Ascribing this behavior to hole emission rather than to electron capture better explains both the observed transient dependence on temperature and the influence of photo-excitation.

The transient signals at dark (fig. III.4.2) peak at a temperature T_m, shifting with the pulse width. For lower temperatures the transient amplitudes rapidly decrease. An Arrhenius plot of the T_m dependence on pulse width t_{OFF} (shown in fig. III.4.3) allows the determination of the activation energy E_A of the generation lifetime. The extracted value of 0.58 eV indicates that the defects acting as generation centers lie close to the middle of the silicon band gap.

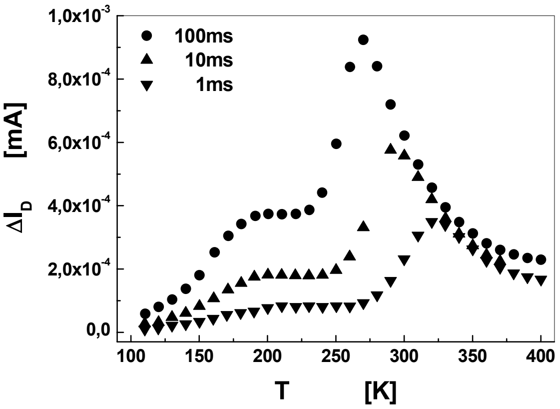


***Fig. III.4.2:** Temperature dependence of transient amplitude for different t_{OFF} durations.*

The value of the generation lifetime activation energy E_A could be used as a measure of the quality of the polysilicon films obtained by various techniques to various thicknesses. Finally, the temperature dependence of the quiescent drain current reveals, as shown in fig. III.4.3, an activation energy of 24 meV at dark and of 12 meV under illumination; this decrease under illumination is caused by the generated photovoltage across the barriers, which results in a decreased potential barrier height.

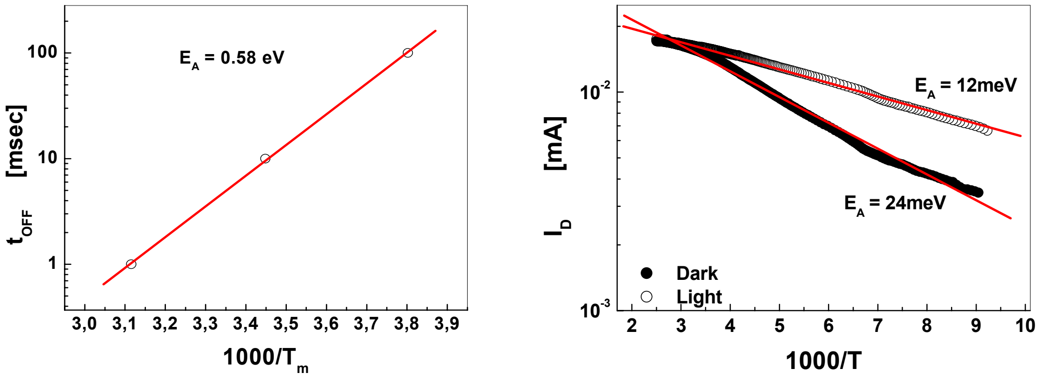


***Fig. III.4.3:** Arrhenius plots of transient signal peak **(left)** and of quiescent I_D **(right)**.*

Task 3 Irradiation investigation

The degradation of the parameters of “directional” polysilicon SLS ELA TFTs under γ-irradiation was investigated and found to be more evident with increasing polysilicon film thickness and in the presence of a gate field during the irradiation. The extracted V_{th} and μ values are presented in fig. III.4.4. The γ-irradiation of these TFTs resulted in positive oxide charge trapping, inducing a negative V_{th} shift. The fact that the mobility was only slightly degraded indicates a good quality of the polysilicon – SiO_2 interface. The large V_{th} shift observed, which reaches 7 V at a dose of 700 Gy, indicates a high sensitivity of the PECVD gate oxide to γ-irradiation. Moreover, the charge trapping ΔN_{ot} in the oxide and ΔN_{it} at the interface was extracted using the shifts in the threshold and the midgap voltage ΔV_{th} and ΔV_{MG} (via the McWhorter – Winokur procedure), as shown in fig. III.4.4, and their increase with rising γ-irradiation dose was determined. It is evident that the irradiation-induced increases of the trapped charge densities ΔN_{ot} and ΔN_{it} are larger for TFTs fabricated in thicker polysilicon films.

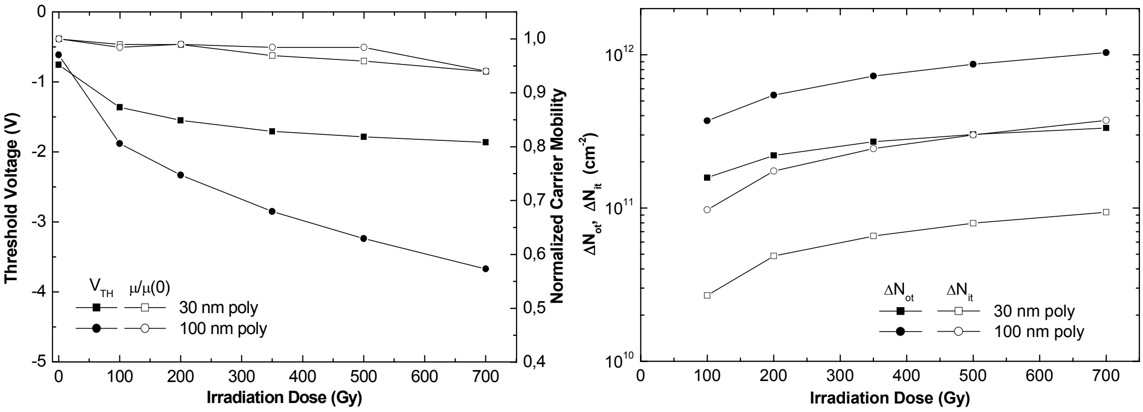


Fig. III.4.4: *V_{th} shift and μ degradation (left) and ΔN_{ot}, ΔN_{it} (right) vs. irradiation dose.*

Task 4 Polysilicon material characterization

The surface morphology and the grain structure of the polysilicon films are observed by means of SEM and AFM, while an investigation of the optical properties as a means for estimating the defectivity of the films has been initiated. The existence of a preferred direction for “directional” SLS ELA polysilicon films is evident from the SEM micrograph shown in fig. III.4.5.

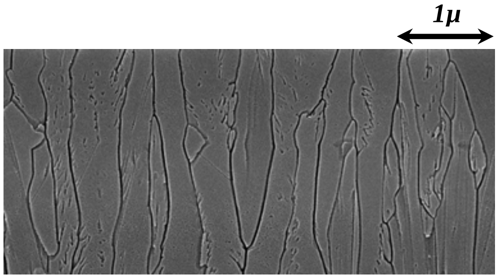


Fig. III.4.5: SLS ELA poly-Si film.

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS

1. "On the switch-on overshoot transient decay mechanism in polycrystalline silicon thin film transistors", Papaioannou, G.J., M. Exarchos, D.N. Kouvatsos and A.T. Voutsas, Applied Physics Letters, 87 (25), 252112, December 2005.
2. "Characterization of various low-k dielectrics for possible use in applications at temperatures below 160ºC", Vasilopoulou, M., S. Tsevas, A.M. Douvas, P. Argitis, D. Davazoglou and D. Kouvatsos, J. of Physics: Conference Series, 10, 218, October 2005.
3. "Effects of DC gate and drain bias stresses on the degradation of excimer laser crystallized polysilicon thin film transistors", Kouvatsos, D.N., L. Michalas, A.T. Voutsas and G.J. Papaioannou, Journal of Physics: Conference Series, 10, 45, October 2005.
4. "Deep Level Transient Spectroscopy Assessment of Drain Current Transients in Poly-Si Thin Film Transistors", Exarchos, M.A., G.J. Papaioannou, D.N. Kouvatsos and A.T. Voutsas, Journal of Physics: Conference Series, 10, 23, October 2005.
5. "The effect of Generation-Recombination mechanisms on the transient behavior of polycrystalline silicon transistors", Papaioannou, G.J., A. Voutsas, M. Exarchos and D. Kouvatsos, Thin Solid Films 487 (1-2), 247, September 2005.
6. "Characterization of various insulators for possible use as low-k dielectrics deposited at temperatures below 200ºC", Vasilopoulou, M., A. Douvas, D. Kouvatsos, P. Argitis and D. Davazoglou, Microelectronics Reliability 45 (5-6), 990, May 2005.
7. "Effect of silicon thickness on the degradation mechanisms of sequential-laterally-solidified polycrystalline silicon thin film transistors during hot-carrier stress", Voutsas, A.T., D.N. Kouvatsos, L. Michalas and G.J. Papaioannou, IEEE Electron Device Letters EDL-26 (3), 181, March 2005.

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. "Effect of hot carrier stress on the performance, trap densities and transient behavior of SLS ELA TFTs", Kouvatsos, D.N., G.J. Papaioannou, M. Exarchos, L. Michalas and A.T. Voutsas, Proceedings of the 35th European Solid State Device Research Conference (ESSDERC 2005), p. 395, Grenoble, France, September 2005.
2. "Thin film transistors fabricated in laser-crystallized chemically vapor deposited amorphous silicon films on quartz substrates", Kouvatsos, D.N., A.T. Voutsas and G.J. Papaioannou, Proceedings of the 15th European Conference on Chemical Vapor Deposition (EuroCVD-15), Bochum, Germany, September 2005.

CONFERENCE PRESENTATIONS

1. "Characteristics of MOS diodes using sputter-deposited W or Cu/W films", Tsevas, S., M. Vasilopoulou, D.N. Kouvatsos, A. Speliotis and D. Niarchos, Micro-and-Nano-Engineering 2005, Vienna, Austria, September 2005.
2. "Investigation of the temperature dependence of the electrical characteristics of polycrystalline silicon thin film transistors", Michalas, L., G.I Papaioannou, D. Kouvatsos & A.T. Voutsas, 21st Panhellenic Conf. for Solid State Phys., Nicosia, Cyprus, Sept. 2005.
3. "Fabrication and characterization of MOS diodes with W or Cu/W gates deposited using sputtering", Tsevas, S., M. Vasilopoulou, D.N. Kouvatsos, A. Speliotis and D. Niarchos, 21st Panhellenic Conference for Solid State Physics, Nicosia, Cyprus, September 2005.

M.Sc. THESIS

1. "Investigation of hot carrier effects in polycrystalline silicon TFTs", Loukas Michalas, Physics Department, University of Athens, January 2005.

PROJECT III.5: CIRCUITS & DEVICES FOR OPTOELECTRONIC INTERCONNECTIONS

Project Leader: Dr G. Halkias
Other Key Researchers: S. G. Katsafouros
PhD Candidates: K. Minoglou
External Collaborators: Dr E.D. Kyriakis-Bitzaros
Research Associates: E. Grivas, P. Robogiannakis

Funding:

- EU-STREP-IST PICMOS, Contract N^o 002131, 1/1/2004-31/12/2006
- OPTOELECTRONICS (ESA) - Multigigabit optical backplane for space applications, Contract N^o 17884, 5/1/2004-4/7/2005

Research orientation:

The main objective of the project is the development of the technologies for future high-density and high-speed optoelectronic interconnections. In order to accomplish this objective the additional specific targets of optoelectronic device modeling and simulation, implementation of optoelectronic technology in spacecraft environment as well as packaging in terms of photonic link integration above CMOS integrated circuits have been identified.

Main results in 2005:

The main results obtained in 2005 within the different tasks of the project are given below.

Task 1 Development of a model for simulating Vertical Cavity Surface Emitting Lasers (VCSELs) and driving circuit topologies

Motivated by the fact that the ability to model VCSEL optical behaviour is critical to the design and analysis of optoelectronic micro-systems, we expand our proposed model scheme so that it will combine the non-linear behaviour of the input parasitics with the intrinsic fundamental device rate equations. The complete model for the VCSEL takes into account, by means of equivalent circuits the fundamental device rate equations, the thermal effects, the non-linear gain and transparency number functions and the input parasitic elements. A systematic methodology for the model parameter extraction from dc and ac, electrical and optical measurements is developed and extraction is achieved by a three-step procedure, which divides model parameters into distinct groups. Simulation results see fig. III.5.1a and b, using the proposed model, is compared with the experimental measurements and present satisfactory agreement. Simulation and extraction procedures are proved to be very fast while they preserve adequate accuracy.

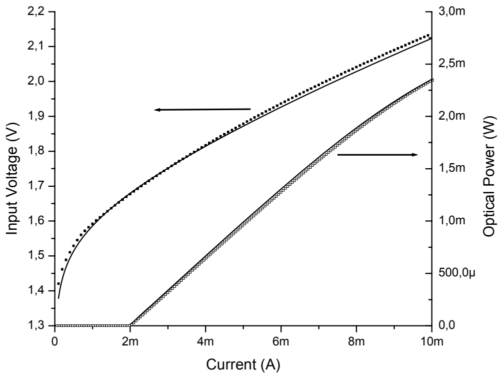


Fig. III.5.1a: *Measured values (dots) & simulated (continuous line) I-V & I-L characteristics at 20ºC*

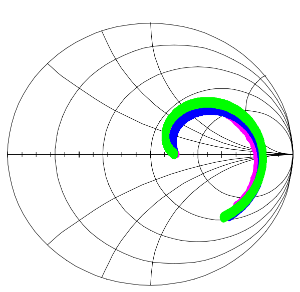


Fig. III.5.1b: *Measured values (pink line) @6mA & simulated s11 using parameters extracted @6mA & @4mA (blue & green line)*

Task 2 Multigigabit optical backplane for space applications

With the changing requirements in satellite operation it is important to assess how current developments in optical backplane interconnections can be applied to the next generation of spacecraft data handling and communication systems. This has been the goal of the ESA project ‘Multigigabit optical backplane interconnections’, in which we cooperate with IMEC of Belgium and Intune Technologies Ltd of Ireland.

Having chosen a wavelength routed star network architecture, based on an arrayed waveguide grating (AWG) router and tuneable transponders in the different nodes a demonstrator was developed. It consists of 4 nodes-of which only two have (for cost saving reasons) sending and receiving capability whereas the other two are only receivers-connected by an optical backplane. The demonstrator basically consists of three parts: the wavelength router, the transponders and the nodes generating or receiving data and implementing the control plane.

- The passive wavelength router transparently implements the network functionality on the physical level. The router has two input ports and four output ports, optically connected to laser and detector ports of the transponders. The router can support unicast and multicast links between inputs and outputs. The wavelength used by a sender determines the receiver of the data sent. A 4x4 AWG has been developed in silicon-on-insulator (SOI) technology, for compactness, and used in the demonstrator.
- The transponder cards contain tuneable transmitter and fixed (APD and PIN based) receiver modules capable of sending and receiving 10Gbps data streams. The transponders are equipped with tuneable laser diodes, which have been equipped with external modulators and control electronics. These lasers have 80 50GHz-spaced wavelength channels from 1528nm to 1563 nm. The switching time for these units is below 100ns for a selected subset of the 80 supported wavelength channels.
- Each transponder communicates electrically with a data and control node that generates 10Gb/s data streams. The nodes also take care of the medium access control using predefined communication schemes locally stored in routing tables on every node. One node acts as the master and provides synchronisation signals to all other nodes in order to change simultaneously to the next backplane configuration. Additionally, all nodes can communicate with a PC. Our work is focused on the protocol aspects of the backplane as well as the design and implementation of the control unit using high-speed FPGAs. In fig. III.5.2 the four-node demonstrator set-up is shown.

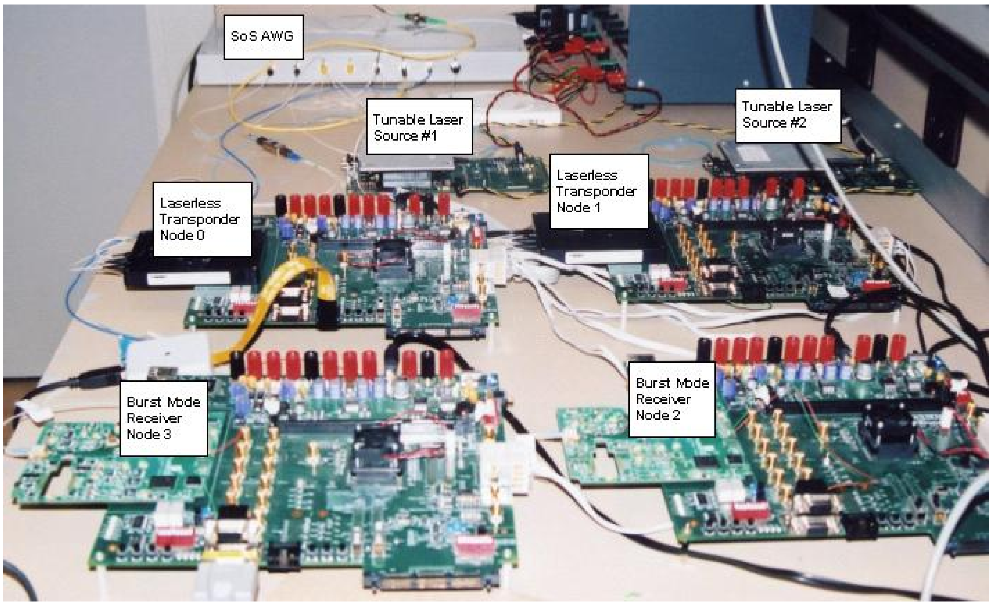


Fig. III.5.2: The Demonstrator Photograph shows the AWG and the 4 nodes: 2 laserless transponders with tuneable laser sources & two burst mode receivers. The four nodes are shown as node 0 to node 3.

Task 3 Heterogeneous integration of optical interconnects onto CMOS ICs

Photonic dies with fully integrated optical paths-sources and detectors coupled to waveguides-are bonded onto a CMOS integrated circuit (IC). The metallic bonding technique that is used utilizes a thin multilayer structure of the Au-20Sn eutectic alloy along with a thin starting layer of rare earth Gd and contains versatile structures for passive alignment. Its main advantage is the fact that it accomplishes mechanical bonding and electrical connectivity in a single step. Pattern uniformity, limited alloy spreading and contact resistance in the mΩ range across a 4-inch wafer allow for dense CMOS/photonic integration. Fig.III.5.3 shows an array of 3x4 dies attached to a 4in wafer. This project is executed in collaboration with IMEC, Belgium, ST, CEA, CNRS-FMNT, France, and TUE, Holland, in the framework of the European project PICMOS.

Fig. III.5.3: *Four-inch wafer with multiple dies bonded on specific regions.*

PROJECT OUTPUT in 2005

PUBLICATIONS in INTERNATIONAL JOURNALS

1. “Driving High Speed VCSELs”, K.Minoglou, E.D. Kyriakis-Bitzaros, S.G.Katsafouros, D. Syvridis, G. Halkias, Microwave and Optical Technology Letters (Vol 44, Issue 1, January 2005, pp. 41-45)

INVITED TALKS

1. “System level modeling and simulation of optical interconnects”, E.D.Kyriakis-Bitzaros, K.Minoglou and G.Halkias, Invited Talk, ECIO’05, 12th European Conference on Integrated Optics, Grenoble, April 6-8 2005, pp.335-344

PUBLICATIONS in CONFERENCE PROCEEDINGS

1. “Metallic bonding of optoelectronic dies to silicon wafers”, K.Minoglou, E.D.Kyriakis-Bitzaros, E.Grivas, S.Katsafouros, A.Kostopoulos, G.Konstadinidis and G.Halkias, Journal of Physics:Conference series 10 (2005), pp.393-396

ANNEX I

RESEARCH PRODUCTS OF IMEL

a) Lithography and plasma etching software

- Software for line-edge-roughness (LER) measurement and characterization from SEM images.
- Software for nanolithography simulation and LER prediction based on Monte Carlo methods.
- Software for topography evolution simulation during plasma processing.

b) MEMs devices

Flow sensors

Using porous silicon micro-hotplate technology, different gas and liquid flow sensors were developed at IMEL. The proprietary gas flow sensor of IMEL using local thermal isolation on silicon either by a compact porous silicon layer or a porous membrane over a cavity, shows superior characteristics compared with other existing devices in the literature.
A system for respiration control using the above flow sensor has been designed and fabricated at IMEL which works quite linearly in a large flow range from -200 to +200 slpm. The system shows important advantages compared with existing systems in the commerce (high sensitivity, low cost, linearity, fast response). Modeling and simulation were used to optimize the sensor and housing design.

Thermal accelerometer based on porous silicon technology for thermal isolation

A silicon accelerometer without solid proof mass has been developed and characterized, based on the thermal sensor developed at IMEL. The device was tested in a specially designed vibration system for different frequencies and acceleration values. It shows important advantages over existing systems also for this application, when used in a fluid medium.

Porous-silicon-sealed microchannels on a silicon substrate

A two-step electrochemical process has been developed for the fabrication of sealed air cavities or capped micro-channels on a silicon substrate. The capping material is a porous silicon membrane which is planar to the silicon substrate. Two interesting applications of this technology are targeted: a) The effective local thermal isolation on a silicon wafer for use in micromachined thermal sensors, b) The potential use of this technology in the fabrication of microfluidic devices. Research in this direction is related with the design, modelling, fabrication and characterization, using the above process.

c) Bio - MEMs

A bioanalytical lab-on-a-chip device based on monolithic optoelectronic transducers has been developed at IMEL (see project III.3).

ANNEX II

ORGANIZATION OF CONFERENCES, WORKSHOPS & PROJECT MEETINGS AT IMEL in 2005

1. Resist issues for EUV lithography Workshop, P. Argitis, Athens, Greece, 05/2005
2. Summer School “Methods in Micro-Nano Technologyand Nanobiotechnology”, 6-10 June 2005. Laboratory courses: “Microfluidics with soft lithography” (A. Tserepi, M. Vlachopoulou), “Microfluidics with Plasma Etching” (E. Gogolides, N. Vourdas)
3. Meetings for the projects CRISPIES in SOARING, E. Gogolides
4. Two meetings of the EU project PROTEAS PV System (Athens 30 September and 20 December 2005)
5. Summer School at NCSR Demokritos, "Orientation and Information on recent developments in Research and Technology", A. Tserepi, 11-22/7/2005
6. Workshop: Nanotechnology meets diagnostics-nanoassays, 7/12/2005
7. MINA-EAST NET Workshop, at NCSR Demokritos, A. G. Nassiopoulou, 15/7/2005
8. Two-day presentation on the progress of post-graduate students of IMEL, 15-16/12/2005 Program:
    - “Fabrication of macroporous silicon and deposition of metals in its pores”, Zacharatos Filimon
    - “Roughness formation during silicon etching using plasma for microfluidic devices”, Boulousis George
    - “Self-assembly of gold nanoparticles between electrodes by dielectrophoresis”, Zoy Argyro
    - “Nano-chromatography and mass-spectroscopy devices for the determination of protein cancer indices in biological liquids”, Zerefos Panagiots
    - “Study of the influence of nitrogen in the electrical characteristics of MOS devices made of silicon under strain”, Kelaidis Nikolaos
    - “Development of methods for deposition of thin organic films with applications in electronic devices”, Tatakis George
    - “Silicon nanocrystals as building blocks for memory devices”, Dimitrakis Panagiotis
    - “Polymeric materials and processes for microlithography in thin films”, Niakoula Dimitra
    - “Processes for patterning PDMS for fabrication of microfluidic devices”, Vlachopoulou Marilena
    - “Fabrication and applications of ultra-thin porous alumina films grown on silicon”, Gianneta Violetta
    - “Technology of lithographic masks for integrated circuits with critical dimension of 65 and 45 nm”, Tsikrikas Nikolaos
    - “Plasma treatment of polymeric materials for fabrication of microfluidic devices”, Bayiati Pinelopi
    - “Growth and chracterization of copper oxide thin films and their application in electronic devices”, Papadimitropoulos George
    - “Porous alumina thin films grown on silicon: fabrication, properties and applications”, Kokonou Maria
    - “Arrays of semiconductor nanocrystals embedded in an insulating matrix for memories”, Olziersky Antonis
    - “Microfluidics for chemical and biological microanalysis. Plasma processing for surface treatment and for fabrication of related devices”, Vourdas Nikolaos
    - “High density integrated optoelectronic circuits for high-rate photonic Microsystems”, Minoglou Kyriaki

ANNEX III

SEMINARS – LECTURES at IMEL in 2005

1. “Single Wall Carbon Nanotubes and Semiconductor Nanocrystals in biosensory applications” by Dr F. Papadimitrakopoulo, Professor of Chemistry Associate Director, Institute of Materials Science, University of Connecticut, USA, 14/01/2005
2. “Advanced Gate Dielectrics”, by Prof. T. P. Ma, Chairman of Department of Electrical Engineering, Yale University, USA, 31/03/2005
3. “Electrical Characterization of shallow InGaAs/InAlAs high electron mobility transistors”, by Dr E. Skouras, Ass. Prof. Depatrment of Materials Science, University of Ioannina, Greece, 20/4/2005
4. “Scanning Probe Techniques for Dopant Profile Characterization” by Dr Maria V. Stagnoni, Federal Institute of Technology (ETH), 19/10/2005
5. “AlInGaN-based Ultra-Violet Light Emitters- Microscopic Physics of Device Operation” by Dr Eleni Makarona (PhD Brown University), 19/10/2005
6. “Electronic Devices based on Thin Organic Films”, by Prof. Mike Petty, Centre for Molecular and Nanoscale Electronics, University of Durham, 27/10/2005
7. “Characterization of materials with surface-sensitive techniques and their application in microelectronics”, S. Kennou, Department of Chemical Engineering University of Patras – ICE/HT-FORTH, Patras

ANNEX IV

PARTICIPATION OF IMEL’s SCIENTISTS IN CONFERENCES

During 2005 IMEL scientists participated in the following Conferences:

1. International Conference on Organic Electronics
2. 2nd International Scientific Conference in Information Technology and Quality,
3. Micro- and Nano-Engineering, MNE
4. Int. Sematech EUVL symposium
5. ACS Pacific Polymer Conference
6. EMAS conference
7. 5th Int. Conf. Polymer Surface Modification
8. 4th Int. Conf. Instrumental Methods of Analysis
9. 15th European Conference on Chemical Vapor Deposition (EUROCVD 15)
10. 20th European Photovoltaic Solar Energy Conference & Exhibition (EUPVSEC)
11. 35th European Solid State Device Research Conference (ESSDERC)
12. 21st Panhellenic Conference for Solid State Physics
13. 3rd International Symposium on Nanofacturing, ISNM
14. SPIE Conference on " Microtechnologies for the New Millenium 2005"
15. CIP
16. 17th International Symposium on Plasma Chemistry, ISPC
17. XXV Dynamics Days
18. 2nd Panhellenic Conference on Plastics,
19. XXI Panhellenic Conference on Solid State Physics and Material Science
20. 1st Panhellenic Conference on Metrology
21. 9th Intern. Conf. On Electromagnetics in Adv. Applications ICEAA
22. First International Workshop on Semiconductor Nanocrystals, SEMINANO
23. International Symposium of Micromanufacturing
24. E-MRS Spring Meeting
25. 1st International Conference on Memory Technology and Design (ICMTD)
26. Eurosensors XIX
27. Nanomeeting
28. 12th European Conference on Integrated Optics

ANNEX V

INFRASTRUCTURE AT IMEL

The infrastructure available at IMEL is unique in Greece and it includes state-of-the art equipment and facilities for both micro and nanofabrication in a clean room area, and for design, modeling, characterization and testing of materials, devices, circuits and systems. A great part of the infrastructure has been funded through competitive projects at National and European level.
The clean room of a total area of $300m^2$ has been fully upgraded in the year 2002.

The infrastructure available at IMEL includes the following:

I. Silicon processing laboratory in a clean room area of 300 m^2, equipped with the following:

- 4 laminar flow chemical benches
- 7 horizontal hot-wall furnace tubes
- 2 horizontal LPCVD tubes for nitride, oxide (TEOS), polysilicon
- 1 horizontal LPCVD tube for LTO
- Ion Implanter (EATON medium current, 200 KeV)
- Optical lithography systems (resolution down to 0,6 µm)
- Electron beam lithography system (resolution 50 nm)
- Reactive Ion Etcher
- Plasma processing system
- Metallization equipment (thermal, e-gun evaporation, sputtering)
- Process inspection equipment

II. Processing equipment not in clean room:

- High Density Plasma Etcher
- Different thin film deposition systems
  - → Sputtering
  - → MOCVD

III. Characterization, Testing and Inspection Equipment

- *Electrical characterization equipment*
  - Karl Suss PA150 semi-automatic probe station
  - Karl Suss manual probe station
  - Micromanipulator probe station
  - HP measuring systems (4142B, 4084B, 8110A, 700i series, 4140B, 4284, 4192A, 34401, 16500A)
  - Keithley measuring equipment (230, 220, 617, 195A, 6517A)
  - Tektronix 224J Oscilloscope
  - Oxford optistat Cryostat for temperatures in the range 4.2-320 K.
  - Oxford DN cryostat for temperatures in the range 77-500 K
- *Optical characterization equipment*
  - Multiwavelength Spectroscopic Ellipsometer
  - FTIR system, model Tensor 27 of Bruker
  - Jobin Yvon spectrometer, wavelengths 300-1600 nm
  - Argon Laser

  - Oxford optistat Cryostat, 4.2-320 K
  - Emission spectroscopy set-up for electroluminescence measurements: USB-2000 spectrometer (Ocean Optics)
- *Morphology, structural characterization*
  - Leo 440 SEM
  - AFM
  - Stylus profilometer model XP-2 of Ambios Technology
- *Testing equipment*
  - Systems for testing of gas flow, gas, pressure, acceleration and humidity sensors.

IV. Modeling/Simulation Software

- *Process and device modeling software*
  - SILVACO Software (Athina, Atlas)
  - Suprem and Pisces
  - Floops and floods
  - Synopsys TCAD Tools
  - Software for MEMs modeling and simulation
  - Coventorware
  - FEM-LAB

V. VLSI Design Facilities

- *Hardware*
  - H-P 9000/ 700
  - SUN Ultra workstations
- *Software from schematic or VHDL to mask layout and verification*
  - Cadence
  - Mentor Graphics
  - Synopsis

ANNEX VI

PERSONNEL

Researchers

1. Nassiopoulou A.G., Director
2. Argitis P.
3. Davazoglou D.
4. Gardelis S.
5. Glezos N.
6. Goggolides E.
7. Halkias G.
8. Ioannou-Sougleridis V.
9. Kouvatos D.
10. Misiakos K.
11. Normand P.
12. Papanikolaou N.
13. Raptis I.
14. Tsamis C.
15. Tserepi A.

Research Engineers

1. Tsoi E.
2. Katsafouros S.

Research Associate

1. Contopanagos H.

Post Doctoral Scientists

from Regular Public Budget

1. Chatzandroulis S
2. Douvas A
3. Goustouridis D.
4. Patsis G.
5. Skarlatos D.
6. Vambakas V.

on Contract

1. Catzichristidi M.
2. Konstandoudis K. .
3. Vassilopoulou M.
4. Pagonis D. N.

PhD Students

from Regular Public Budget

1. Bayatti P.
2. Chaidogiannos G.
3. Chronaios A.
4. Kelaidis N.
5. Κοκονού M.

PhD Students

6. Minoglou K.
7. Olzierski A.
8. Niakoula D
9. Papadimitropoulos G.
10. Polymenakos S.
11. Vlachopoulou M
12. Vourdas N.

on Contract

1. Dimitrakis P.
2. Gianetta V.
3. Grivas E.
4. Kokoris G.
5. Koliopoulou S.
6. Kotsovos K
7. Salonidou A.
8. Zacharatos F.
9. Zoi A.

Scientists on contract

1 Robogiannakis P.

Technical and Administrative Personnel

from Regular Public Budget

1. Lagouvardou M.
2. Makridi Z.
3. Makridis Z.
4. Mavropoulis I.

on Contract

1. Bolomiti E.
2. Boukouras K.
3. Georgiou C.
4. Karmpadaki M.
5. Linarakis E.
6. Sergis E.
7. Tokpasidou E.

ANNEX VII

RESEARCH PROJECTS in 2005

A. EU Projects

- **MICROPROTEIN (STREP-NMP-FP6) –** G5RD-CT-00744
  "Micrometer Scale Patterning of Protein and DNA Chips"
  Duration 1/5/2002 – 31/10/2005, Project leader: P. Argitis

- **SOARING (STREP-IST-FP6) -** Contract No 35254
  "Development and Validation of Source, Optics and Resist in Next Generation EUV Lithography"
  Duration: 1/3/02-28/2/05, Project leader : E. Goggolides

- **PROTEAS (STREP-ENERGY-FP6) -** Contract No ENK6-CT-2002-00674
  "PROTEAS PV System"
  Duration: 1/1/2003-31/12/2005, Project leader: D. Davazoglou

- **SINANO (NoE-IST-FP6) -** Contract No 506844
  "Silicon based Nanodevices"
  Duration: 1/1/2004-31/12/2006, Project leader: A. G. Nassiopoulou

- **GOOD-FOOD (IP-IST-FP6) -** Contract No 508774
  "Food Safety and Quality Monitoring with Microsystems"
  Duration: 1/1/2004-30/6/2007, Project leader: C. Tsamis, A. G.Nassiopoulou

- **PICMOS (STREP-IST-FP6)** Contract No 002131
  "Photonic Interconnet Layer on CMOS by Wafer-Scale Integration"
  Duration: 1/1/2004-31/12/2006, Project leader: G. Halkias

- **MORE-MOORE (IP-IST-FP6) -** Contract No 507754
  "Exploring new limits to Moore's law"
  Duration: 1/1/2004-31/12/2006, Project leader: E. Goggolides

- **OPTOELECTRONICS (ESA European Space Agency) -** Contract No 17884
  "Multigigabit optical backplane interconnections"
  Duration: 5/1/2004-4/7/2005, Project leader: G. Halkias

- **UNINANOCUPS (STREP-NMP-FP6) -** Contract No MRTN-CT-2003-504233
  "Unidirectional nanoscale supramuleculawires assembled by photo – and electro-active metallocyclodextrine cups"
  Duration: 1/1/2004-31/12/2007, Project leader: N. Glezos

- **NANO2LIFE (NoE-NMP-FP6)** Contract No 500057
  "Unidirectional nanoscale supramuleculawires assembled by photo – and electro-active metallocyclodextrine cups"
  Duration: 1/2/2004-31/1/2008, Project leader: K. Misiakos

- **MINA-EAST (NoE-IST-FP6) -** Contract No 510470
  "Micro and Nanotechnologies going to Eastern Europe throuth Networking"
  Duration: 1/5/2004-30/4/2006, Project leader: A. G. Nassiopoulou

- **TASNANO (STREP-NMP-FP6) -** Contract Nr 516865
  "Tools and Technology for the Analysis and Synthesis of Nanostructures"
  Duration: 1/1/2005-31/12/2007, Project leader: N. Glezos

- **MARIE-CURIE "Re-integration grant (FP6)" -** Contract No 016142
  "Convergence of Microelectronics, Nanotechnology and High Frequency RF engineering (CMNHFRF)"
  Duration: 29/7/2005-28/7/2007, Project leader : A. G. Nassiopoulou

B. Other International projects

- **Photothermal project (Research agency-Cyprus)**
  "Towards a safe hydrogen production: Photothermal analysis at the limits of parts per trillion"
  Duration: 1/7/2004 – 30/6/2006, Project leader: A. G. Nassiopoulou

C. Contracts with Industry

- Contract with **Remon Medical** (Israel) on pressure sensors development
  Duration:1/6/01-31/5/02 (31/12/2006), Contract: "Pressure sensors development"
  Project leader: D. Tsoukalas (P.Normand)

- Contract with the company **INTEL** "Mol –EU",
  Duration: 1/5/03 - 30/4/06, Project leader: E. Goggolides

- Contract with the company **SHARP**
  "Analysis of TFT and gated Hall devices by DLTS method to clarify type and quantify density of defect-states present in the device active-layer"
  Duration : 1/10/03 - 30/9/05, Project leader : D. Kouvatsos

- Contract with the company **PHOTRONICS**
  "Simulation tool and theoretical calculation of the proximity correction parameters for the e-beam patterning of EUVL masks"
  Duration: 1/6/04 - 30/4/06, Project leader : N. Glezos

- Contract with the company **UNILEVER U.K**.
  "Flow system for Unilever"
  Duration: 1/12/05 - 31/5/07, Project leader: A. G. Nassiopoulou

- Contract with the company **ST Microelectronics** SA, France
  "Microporous silicon and porous alumina grown electrochemically on silicon substrates applied to the fabrication of passive components and nanoelectronic devices"
  Duration: 30/7/ 05 - 30/7 /08, Project leader: A. G. Nassiopoulou

D. Projects funded by GSRT

- **Excellence** fund for:
  "A center of excellence in Micro and Nanotechnologies at IMEL"
  Duration : 1/4/02 - 31/3/06, Project leader : A. G. Nassiopoulou

- **GSRT- PEPER-100B**
  "Wireless subscriber connection in advanced public electrocommunication networks implemented with systems on chip (wireless-mile)"
  Duration: 1/1/04-30/6/06, Project leader : S. Katsafouros

- **GSRT- PENED-03ED579**
  "Macroporous silicon and anodic porous alumina on silicon for integrated RF components and nanoelectronics"
  Duration: 15/7/2005-14/7/2008, Project leader : A. Nassiopoulou

- **GSRT- PENED-03ED276**
  "Critical sub-100 Industrial scale Patterns for CMOS - NANO Architectures' (CMOS-NANO)
  Duration: 1/12/2005 – 30/11/2008, Project leader : I. Raptis

- **GSRT- PENED - 03ED550**
  "Development of polysilicon TFT technology with advanced techniques of film annealing and device characterization"
  Duration: 15/12/2005 - 14/12/2008, Project leader: D. Kouvatsos

- **GSRT- ENTER-05 EP032**,
  "Development of MOSFET type chemical sensors for wireless sensor networks"
  Duration: 1/12/2005 - 1/12/2007, Project leader: C. Tsamis

- **GSRT- PENED-03ED630**,
  "Micromachined chemical sensors for controlling food safety and quality"
  Duration: 1/11/2005 - 1/11/2008, Project leader: C. Tsamis

- **GSRT- PENED-03ED496**,
  "Dopant diffusion and activation in Group-IV semiconductors (Strained Silicon and Germanium) for novel nanoelectronic devices"
  Duration: 1/11/2005 - 1/11/2008, Project leader: C. Tsamis

- **GSRT- PENED-03ED202**,
  "Fabrication, Properties, and Actuation Technologies for Microfluidic Devices"
  Duration: 1/12/05-31/112008, Project leader: A. Tserepi

E. Bilateral projects

- **Bilateral project (Greece - Czech Republic) - GSRT**
  "Construction of novel electronic ant optical switches based on quantum transport phenomena in molecular nanostructures"
  Duration: 29/7/03 – 28/7/2005, Project leader: N. Glezos

- **Bilateral project (Greece-Poland) - GSRT**
  “Pattern repication in thin polymeric films with novel lithographic approach”
  Duration: 29/6/2004 – 29/6/2006, Project leader: I. Raptis

- **Bilateral project (Greece-Hungary) - GSRT**
  “Development of negative resist polymers for proton beam micromachining and other lithography processes”
  Duration: 1/1/2005 – 31/12/2006, Project leader: I. Raptis

- **Bilateral project (Greece-Yugoslavia) - GSRT**
  “Performance, stress degradation and reliability characterization of thin film transistors for the investigation of defects in polycrystalline silicon films "
  Duration: 5/11/2004-5/11/2006, Project leader: D. Kouvatsos

- **Bilateral project (Greece-Romania) - GSRT**
  “Drug delivery system based on microreservoirs array with porous silicon resorbable membrane caps"
  Duration: 1/2/2006-31/3/2008, Project leader: A. G. Nassiopoulou

IMEL in FIGURES

	TOTAL NUMBER (2005)	NUMBER / RESEARCHER (2005)
PUBLICATIONS in INTERNATIONAL JOURNALS and REVIEWS	54	3.6
PUBLICATIONS in CONFERENCE PROCEEDINGS	51	3.4
INVITED TALKS	14	0.9
CONFERENCE PRESENTATIONS	50	3.33
CITATIONS THIRD PARTY	665	44.33
PATENTS GRANTED in 2005	3	
PANTENT APPLICATIONS in 2005	3	
PhD THESES AWARDED IN 2005	6	
MSc THESES	14	
DIPLOMA THESES	7	